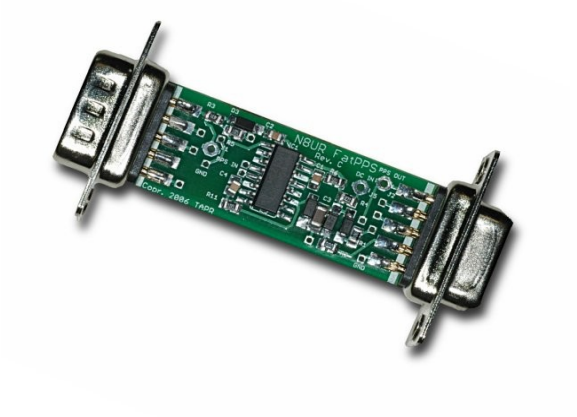
FatPPS Installation and Operation Manual

Pulse Stretcher

Revised: 7 January 2007



Introduction

The TAPR FatPPS is a device that provides an interface between a personal computer serial port and the pulse-per-second ("PPS") signal that is provided by time sources such as GPS receivers and frequency standards. The width of the PPS signal is often very short (sometimes only a few microseconds) and the serial port hardware may not be able to reliably detect these pulses. The FatPPS triggers on pulses as short as 20 nanoseconds and stretches them out to at least 30 milliseconds, which is enough to reliably work with nearly any serial port. The delay between the trigger input and the leading edge of the output pulse is typically 50 nanoseconds or less.

The FatPPS has a male DB-9 connector on its input, and a female DB-9 on its output, so it can be put in series with a normal serial cable. The TXD and RXD signal lines pass through unaltered. The FatPPS can be installed in a plastic "dongle" case, or, if space permits, may be mounted directly in the computer. It can be powered from the computer serial port, and requires no external connections. However, for flexibility solder terminals are provided for DC input (from 5 to 15 volts), PPS input, PPS output, and ground. If using external power, please review the discussion of the power supply circuit below; it may be appropriate to change a resistor value depending on the supply voltage.

The FatPPS input signal can be either positive- or negative- going, and the voltage can be at either TTL or RS-232 levels. The output can be either positive- or negative- going and is a TTL compatible signal which will work with virtually all modern serial port hardware. A solder jumper on the board allows input and output polarity selection.

Important note: Most time sources use the leading edge of the PPS signal for their "on time" marker. The width of the pulse is usually not guaranteed, and selecting an input configuration that results in the FatPPS triggering on the trailing edge may result in poor performance. Similarly, only the leading edge of the FatPPS output signal should be used; the pulse width and therefore the timing of the trailing edge is subject to temperature and other variations and should not be relied upon.

Circuit Description

The FatPPS uses a 74HC123 dual monostable multivibrator chip to implement a pulse stretching circuit.

Power for the '123 is normally provided by the DTR (pin 4 on a DB-9) and RTS (pin 7) signals from the host computer. Most serial ports can source a few milliamps on these lines, and that is enough to power the circuit. R1 and R2 are installed as zero ohm jumpers because most modern serial ports have very limited drive capability. If using the FatPPS with a serial port that provides very "stiff" 12 volt signals on the DTR and RTS lines, it may be appropriate to change those resistors to a higher value (perhaps 470 ohms) to provide current limiting. Diodes D1 and D2 isolate the signals from one another as well as protect the circuit from reverse voltage. If power from the serial port is not available, DC from 5 to 15 volts may be provided to J5. The power source is regulated to 5.1 volts by zener diode D4. 2.2uF capacitor C3 provides a little "flywheel" effect to hold the voltage during peak current drain, and C2 provides decoupling at the IC input.

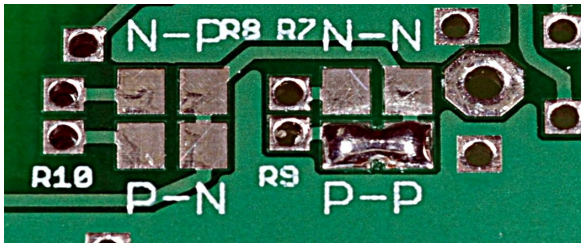
The unofficial standard for interfacing PPS signals to PC computers is to use the Data Carrier Detect ("DCD" and pin 1 on a DB-9 connector) line for this purpose. The input PPS signal therefore arrives on pin 1 of J3 (or alternatively on J1). Resistor R3 provides current limiting and zener diode D3 clamps the signal at +5.1 volts and -0.7 volt to protect the IC. 1 megohm resistor R5 provides a load to prevent the IC's inputs from floating when no signal is present.

Most PPS signals are positive going, but if a true RS-232 drive is used (as is the case, for example, in Z3801A GPS disciplined oscillators), the signal will rest at a positive voltage and go to several volts negative on the leading edge of the pulse. Zener diode D3 clamps any negative signal at about -0.7 volts, which the 74HC123 can safely absorb. Thus, either a TTL or an RS-232 level signal can safely be applied to the FatPPS input.

The 74HC123 provides two multivibrator sections. IC1A is configured to trigger on a negative-going input pulse (*i.e.*, a signal that is normally at +5 volts and reduces to approximately 0 volts on the leading edge). Normal and inverted outputs are on pins 13 and 4 respectively. IC1B is configured to trigger on a positive-going input pulse (*i.e.*, one that goes from 0 to 5 volts on the leading edge). Pins 5 and 12 provide its normal and inverted outputs.

C1 and R6 establish the time constant for the output pulse width for IC1A; C4 and R11 establish the IC1B time constant. According to the formula in the 74HC123 data sheet (Td = 0.45*Rx*Cx), the default values of 1 megohm and 0.1uF should yield a pulse width of about 45 milliseconds. In practice, the pulse width seems to be somewhat shorter and normally is about 30 milliseconds long. If a longer time constant is required, the values of these components may be increased.

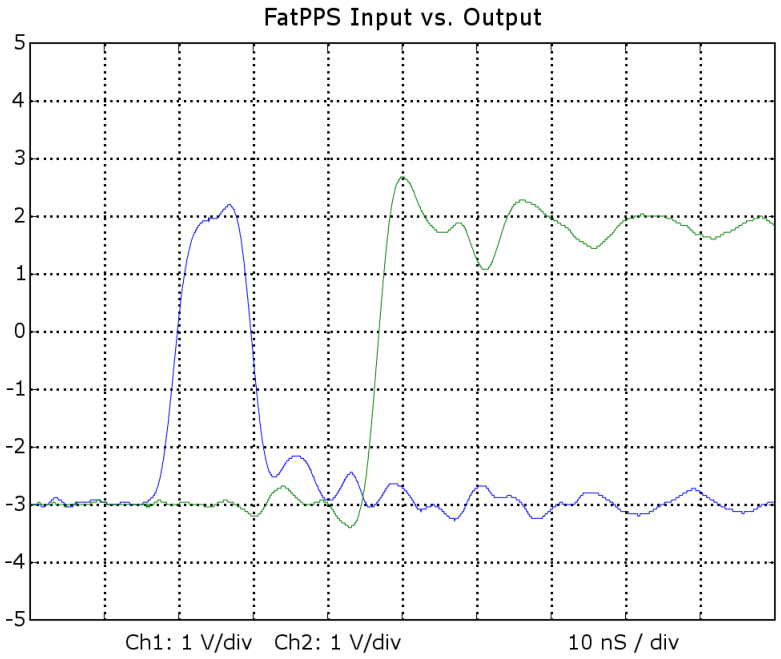
The desired output configuration is selected by installing one (and only one!) of R7-R10. Rather than using a zero ohm resistor which might be difficult to install or remove, assembled boards use a small solder blob. To change configuration, use solder wick to remove the existing short and create a solder bridge across the desired pair of pads. The output signal is routed to pin 1 of J4 as well as to J2. By default, the FatPPS is configured for a positive-going input and positive-going output as shown below.



The RXD and TXD signals on the input connector (pins 2 and 3) are routed directly through to the output connector, so normal serial communications without hardware handshaking are not affected by the FatPPS.

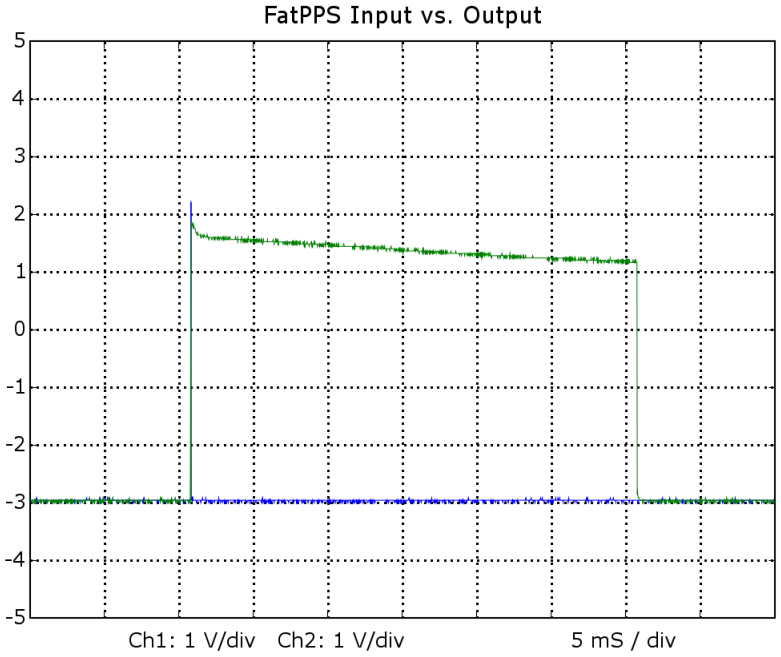
Typical Performance

The FatPPS can be triggered from input pulses of 50 nanosecond or shorter duration. Here is an example:

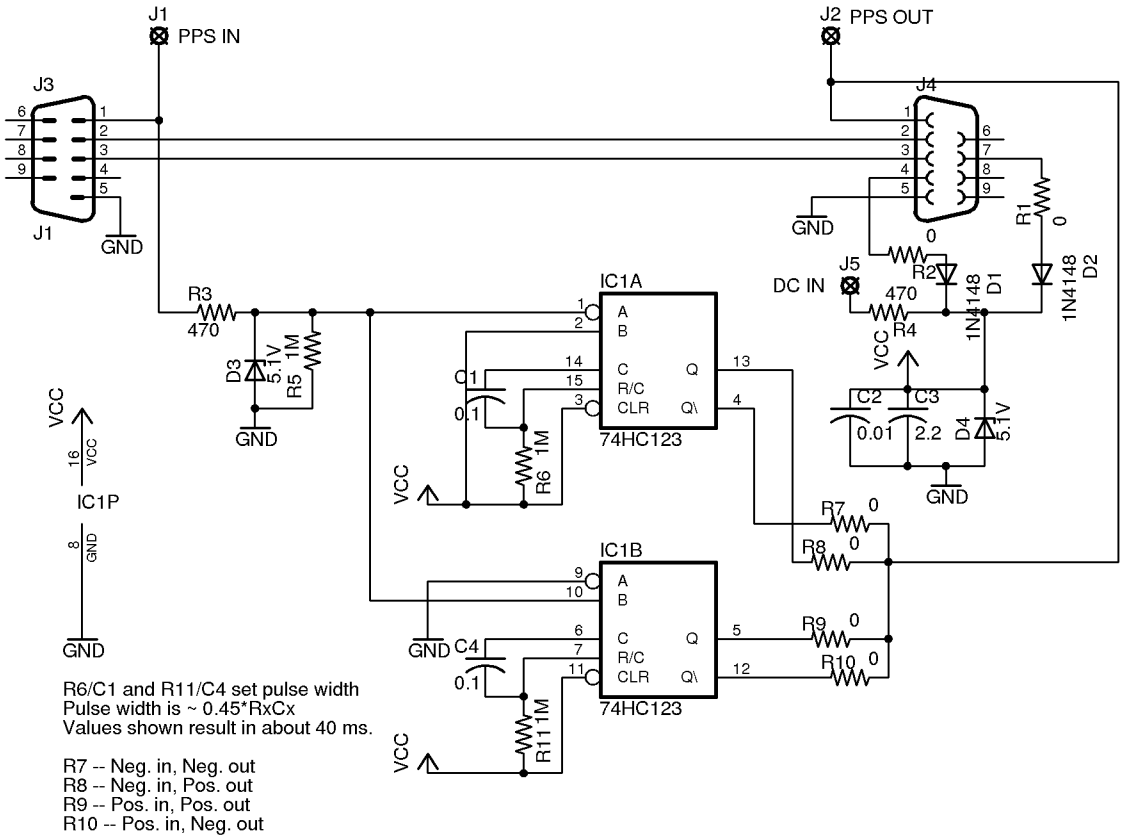


Note that the propagation delay from the rising edge of the input to the rising edge of the output is about 25 nanoseconds. (The transient response of this plot is limited by the 100 MHz digital oscilloscope being used).

This is the output waveform using stock values for the timing components:



The output pulse is about 30 milliseconds long.



R6/C1 and R11/C4 set pulse width
Pulse width is ~ 0.45*RxCx
Values shown result in about 40 ms.

R7 -- Neg. in, Neg. out
R8 -- Neg. in, Pos. out
R9 -- Pos. in, Pos. out
R10 -- Pos. in, Neg. out

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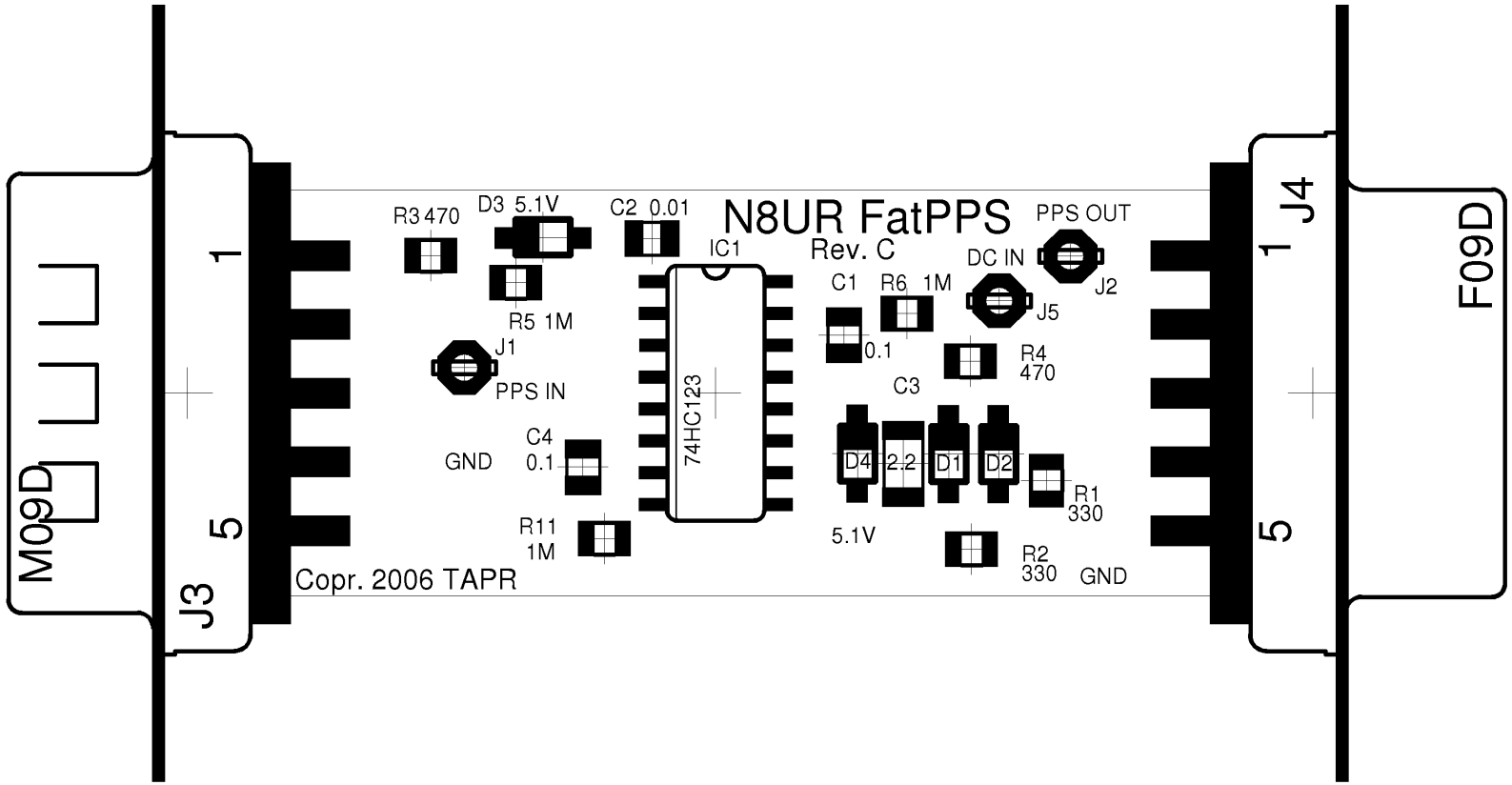
M09D
J3
1
5
F09D
J4
1
5
N8UR FatPPS
Rev. C
PPS OUT
J2
DC IN
J5
R3 470
D3 5.1V
C2 0.01
IC1
74HC123
C1
R6 1M
0.1
R4
470
C3
R5 1M
J1
PPS IN
C4
0.1
GND
D4
2.2
D1
D2
R1
330
R11
1M
5.1V
R2
330
GND
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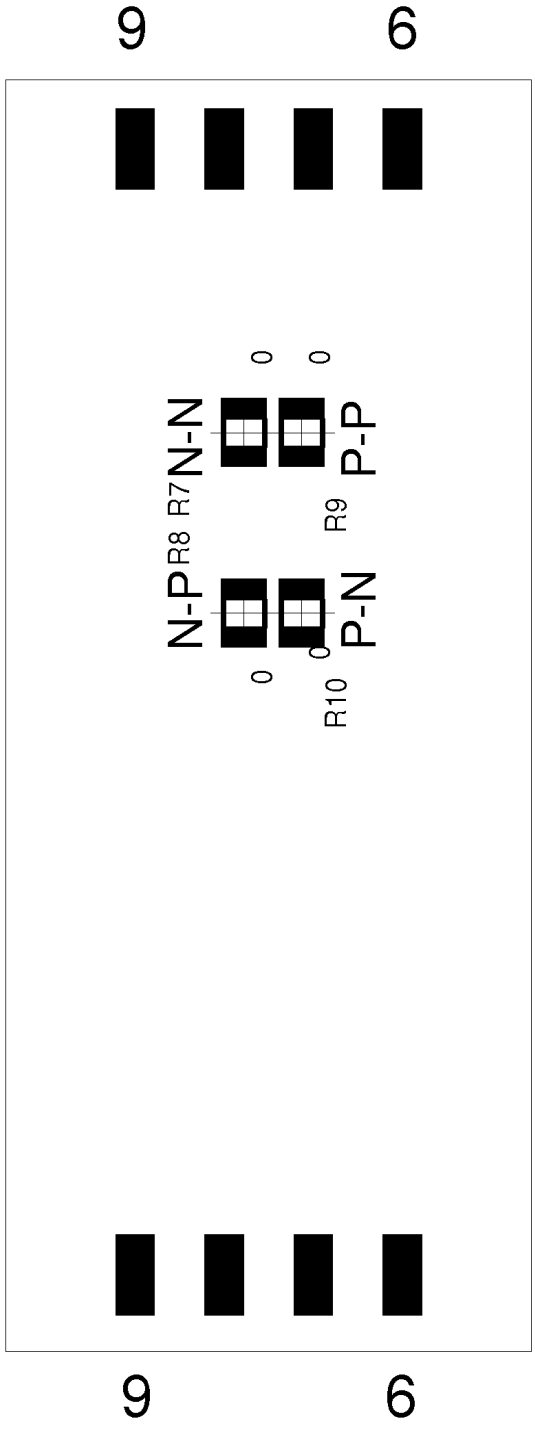
9
6
0
0
N-N
P-P
R7
R8
R9
N-P
P-N
0
0
R10
9
6