the clock line is released by the receiver. The open-drain feature is also needed if this PIC will ever become an I²C slave to another PIC, in which case it must relinquish control of the SCL line.

Figure 9.2 also illustrates that the first eight data bits on the SDA line are sent by the transmitter, whereas the ninth acknowledge bit is a response by the receiver. For example, when the PIC sends out a chip address, it is the transmitter, while every other chip on the I²C bus is a receiver. During the acknowledge bit time, the addressed chip is the only one that drives the SDA line, pulling it low in response to the master’s pulse on SCL, acknowledging the reception of its chip address.

When the byte transfer represents data being returned to the PIC from a peripheral chip, it is the peripheral chip that drives the eight data bits in response to the clock pulses from the PIC. In this case, the acknowledge bit is driven in a special way by the PIC, which is serving as receiver but also as bus master. If the peripheral chip is one that can send the contents of successive internal addresses back to the PIC (e.g., a serial EEPROM), then the PIC completes the reception of each byte and signals a request for the next byte by pulling the SDA line low in acknowledgment. After any number of bytes have been received in this way from the peripheral, the PIC can signal the peripheral to stop any further transfers by not pulling the SDA line low in acknowledgment.