

Modern DSP Tools for Amateur Operations

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AE5JI

37th ARRL and TAPR Digital Communications Conference

September 14-16, 2018 | Albuquerque, New Mexico



Presentation Philosophy

- The world of software defined radio (SDR) and digital signal processing (DSP) is vast and exciting.
- I can't fully address DSP in a 50 min talk – there is *way* too much information to cover.
- Instead, I want you to leave with an understanding of what is possible and the resources to learn more
- Disclaimer: All opinions expressed in this presentation are solely the author's and do not represent those of my employer



Ettus USRP E310 Software Defined Radio
Source: <https://www.ettus.com/product/details/E310-KIT>



Modern DSP Tools for Amateur Operations: Outline

- Scientific applications of high-performance DSP
- Why software defined radio / digital signal processing?
- ADC Basics
- Traditional & Software Defined Radios
- Signal Processing
- Practical DSP: Theory and Implementation
 - Prototyping Languages (SciPy, MATLAB, Lua, GNU Radio)
 - High performance Languages (C++)
 - Computational Accelerators (GPUs, FPGAs)
- Ham Applications



Key takeaways

- The move from analog to digital is going to increase
 - This is a good thing for HAMS!
- Analog design / performance is still very important
- Latency is an issue with general purpose computers
 - FPGAs are needed for low latency applications
- Design tools, development environments, and compilers are increasingly available as free & open source



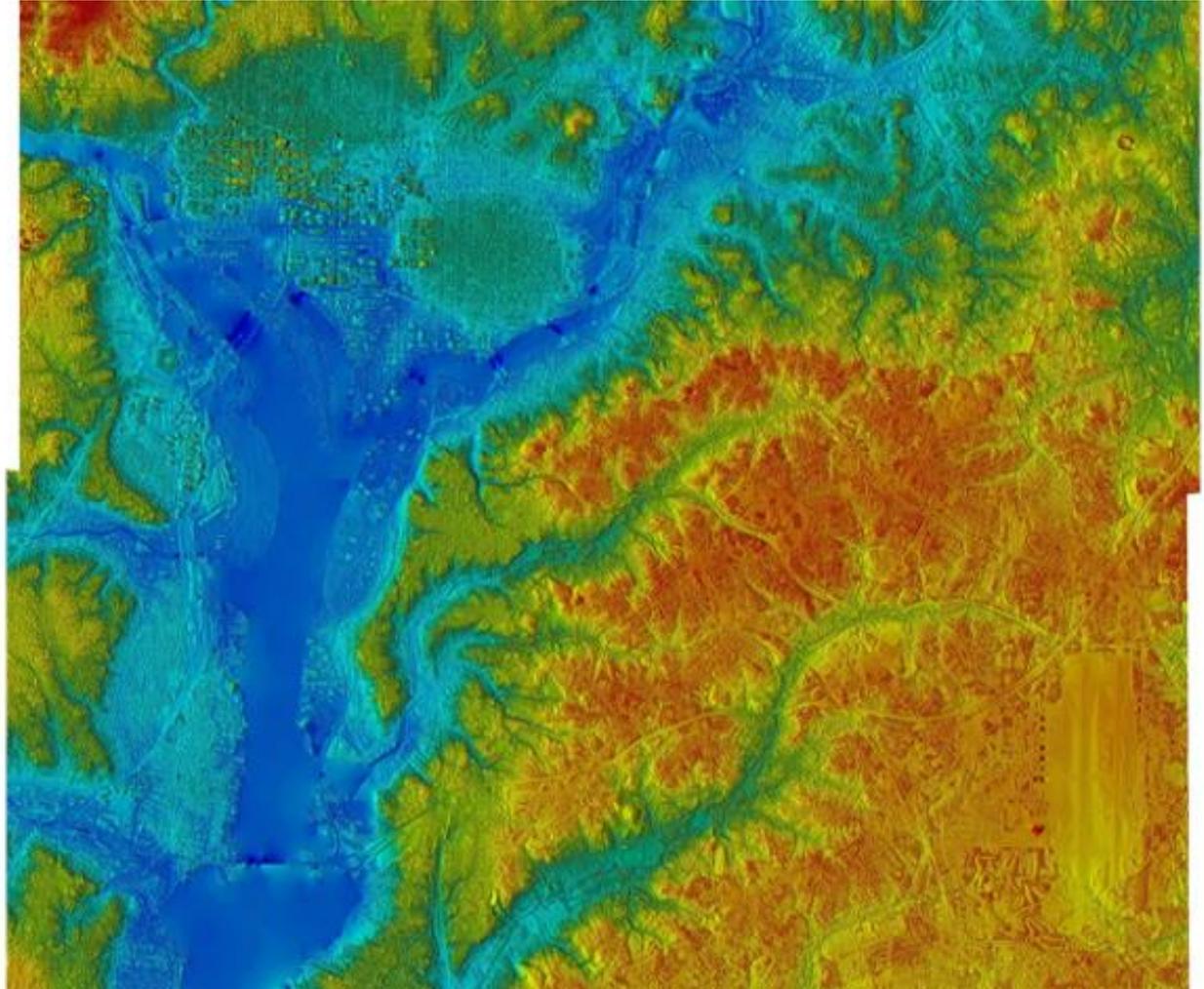
Scientific applications of high-performance DSP

Terrain Mapping

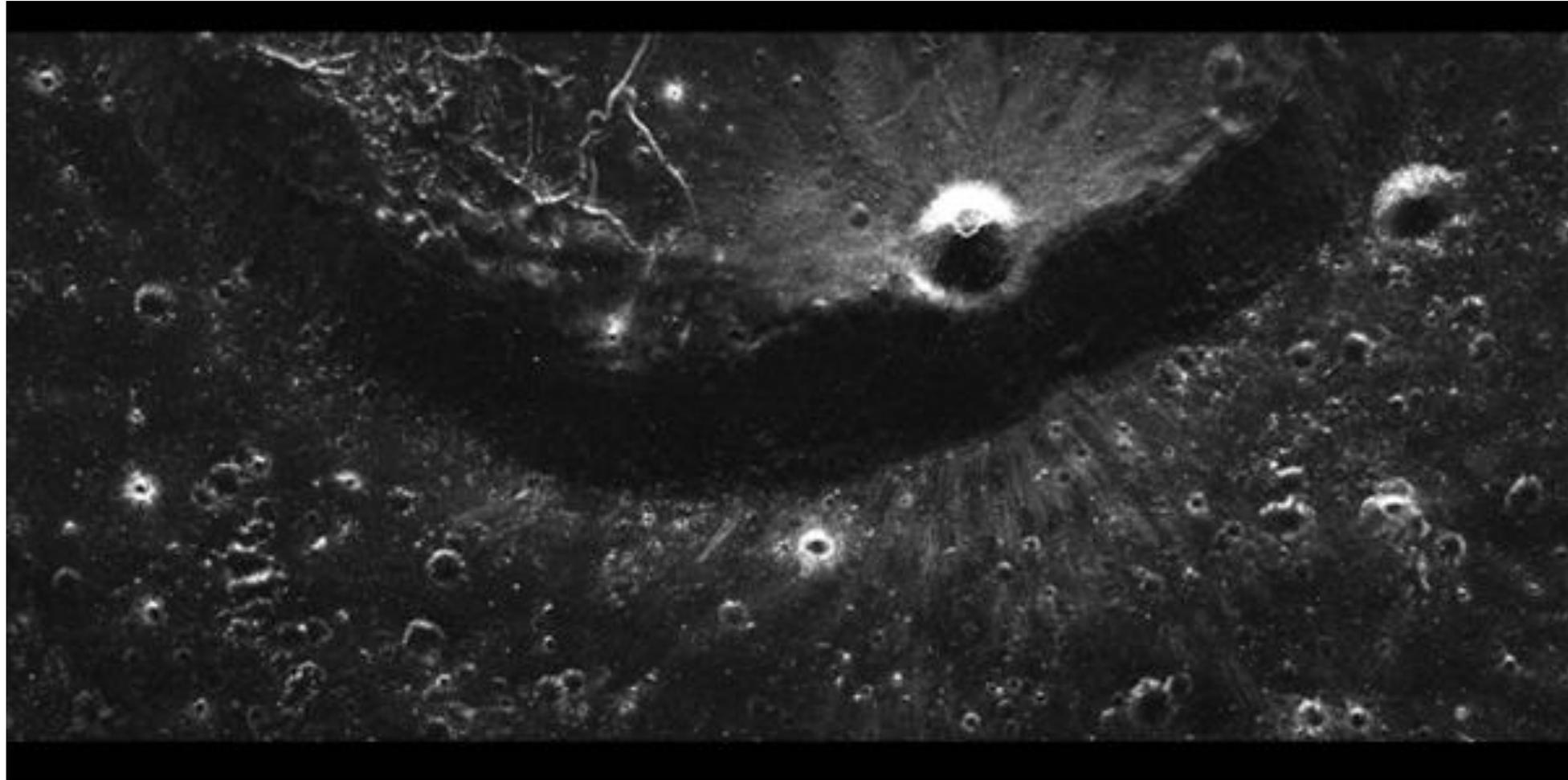
Interferometric Synthetic Aperture Radar (IFSAR) mosaic of greater Washington, DC area from Sandia's Rapid Terrain Visualization (RTV) program.

Source:

<http://www.sandia.gov/radar/imagery/index.html>



Bistatic (SAR) image from Lunar Reconnaissance Orbiter



Bistatic Synthetic Aperture Radar (SAR) image from Sandia's Mini-RF on board the Lunar Reconnaissance Orbiter (LRO).

Source: <http://www.sandia.gov/radar/imagery/index.html>

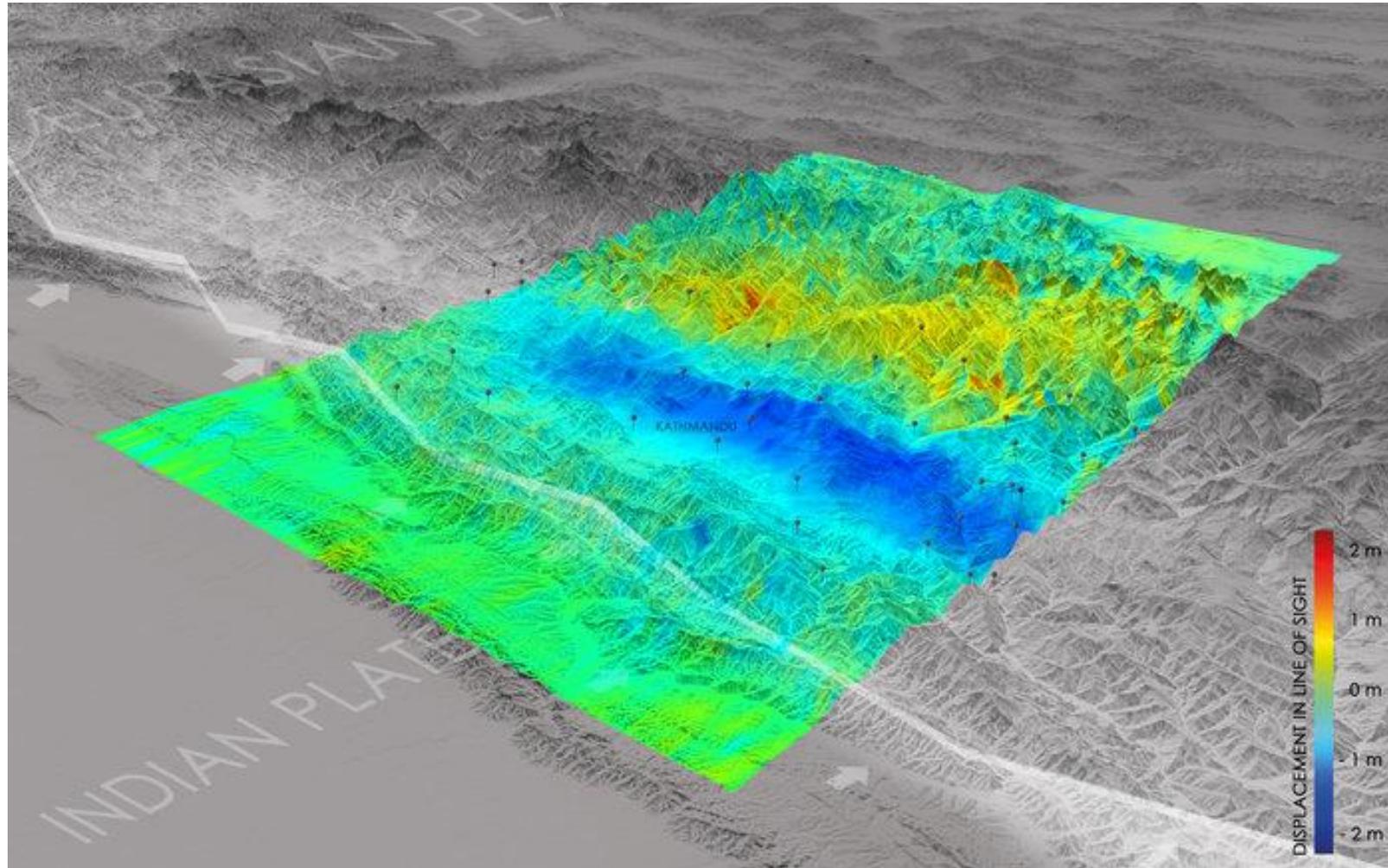
Copernicus Sentinel-1

- European civil space mission
- Pair of SAR satellites
- Near complete coverage of earth land surfaces with 12-day repeat cycle
- Data is freely available online
 - <https://sentinel.esa.int/web/sentinel/sentinel-data-access/access-to-sentinel-data>



Source:
http://www.esa.int/Our_Activities/Observing_the_Earth/Copernicus/Sentinel-1/Facts_and_figures

Copernicus Sentinel-1: Nepal earthquake displacement



Source: http://www.esa.int/spaceinimages/Images/2015/04/Nepal_earthquake_displacement

Why software defined radios /
digital signal processing?



Why digital?

- Digital cost / function rapidly dropping vs. constant analog cost
- They allow component reuse and design standardization
 - Economy of scale is a HUGE price influence in electronics design
- SDRs *may* be reprogrammable to allow future improvements in design
- Newer ICs have lower supply voltages – an issue for analog designs



World class performance in a commodity product

- >2.5 GHz analog bandwidth now available as a commodity product
- Available from many vendors, an example is the XU-TX by Innovative Integration
 - Two, 5 GSPS, 16-bit DACs, 4.8GHz PLL, Xilinx UltraScale FPGA with 4 GB DDR4 Memory



Source: <https://www.innovative-dsp.com/products.php?product=XU-TX>



SDR: Low barrier to entry

- RTL-SDR
 - SDR Receiver for \$8
 - Active development community at <http://www.rtl-sdr.com/>
 - Originally marketed as a tuner for European DVB digital TV
 - R820T2+RTL2832U
 - 3MHz bandwidth with a center frequency from 24 – 1766 MHz



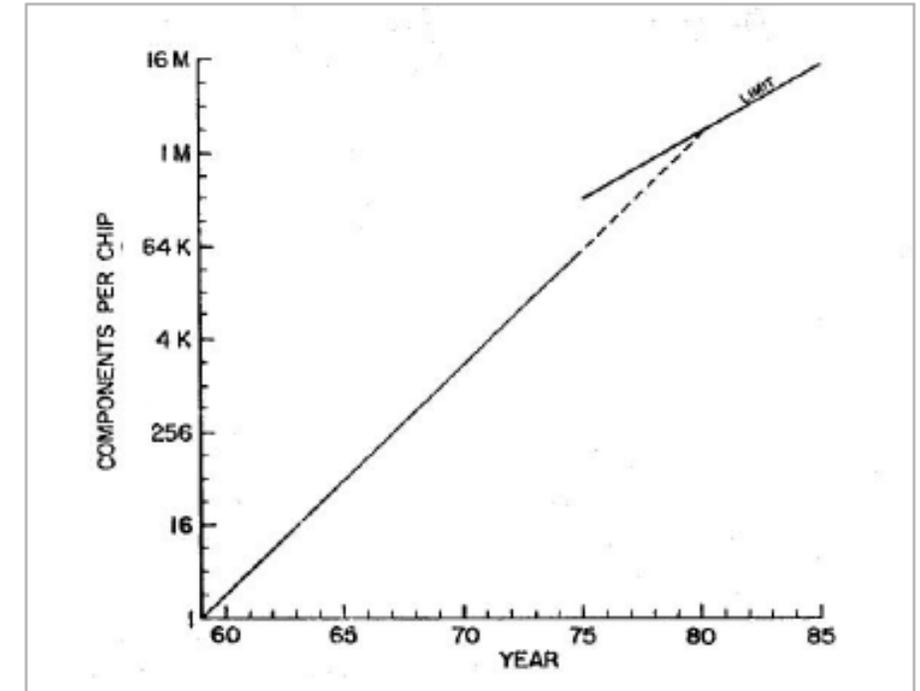
Source: <http://www.amazon.com>

Moore's Law

IC transistor density will on average double every 2 years

“With this factor disappearing as an important contributor, the rate of increase of complexity can be expected to change slope in the next few years as shown in Figure 5. The new slope might approximate a doubling every two years, rather than every year, by the end of the decade.”

Figure 5 Projection of the complexity curve reflecting the limit on increased density through invention.



Source: [3] <http://ieeexplore.ieee.org/iel5/9941/31745/01478174.pdf>

[1] Moore, Gordon E. "Cramming More Components Onto Integrated Circuits, Electronics,(38) 8." (1965).

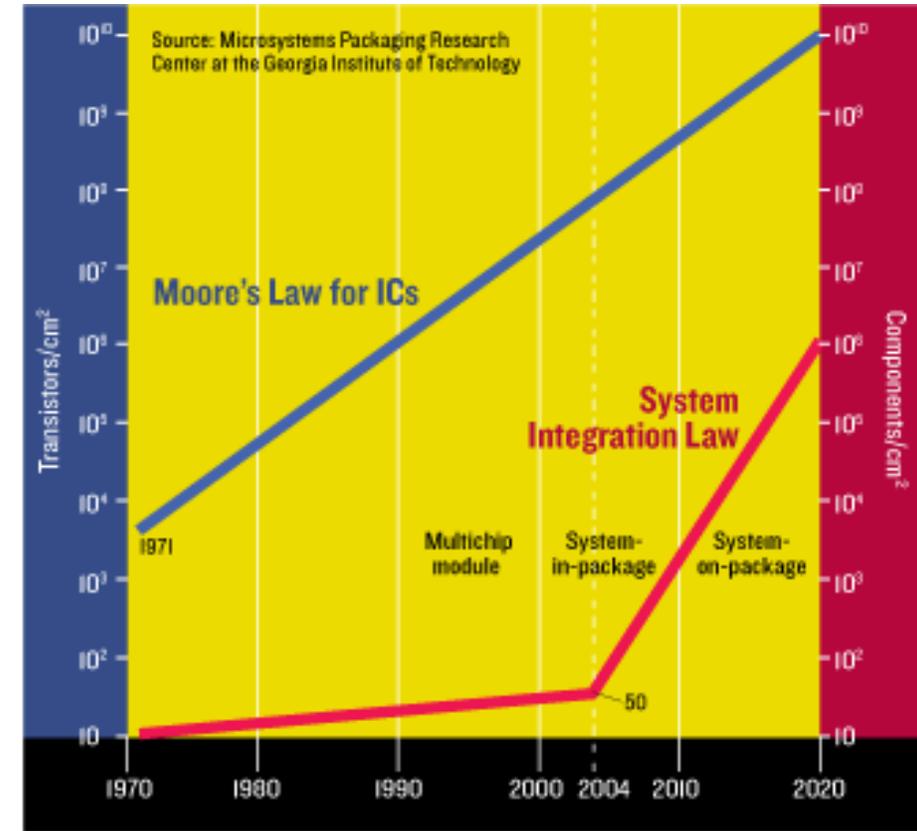
[2] Moore, Gordon E. "Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965, pp. 114 ff." *IEEE Solid-State Circuits Society Newsletter* 20.3 (2006): 33-35.

[3] Moore, Gordon E. "Progress in digital integrated electronics." *Electron Devices Meeting*. Vol. 21. 1975.



Other “Moore’s Law” like factors

- Improvements in oscillators
 - Driven largely by the world wide cell phone market (>5 billion active GSM subscribers)
- Improvements in analog-to-digital converters (ADC)
- Increase in complexity of systems on a chip (SoC) [1]



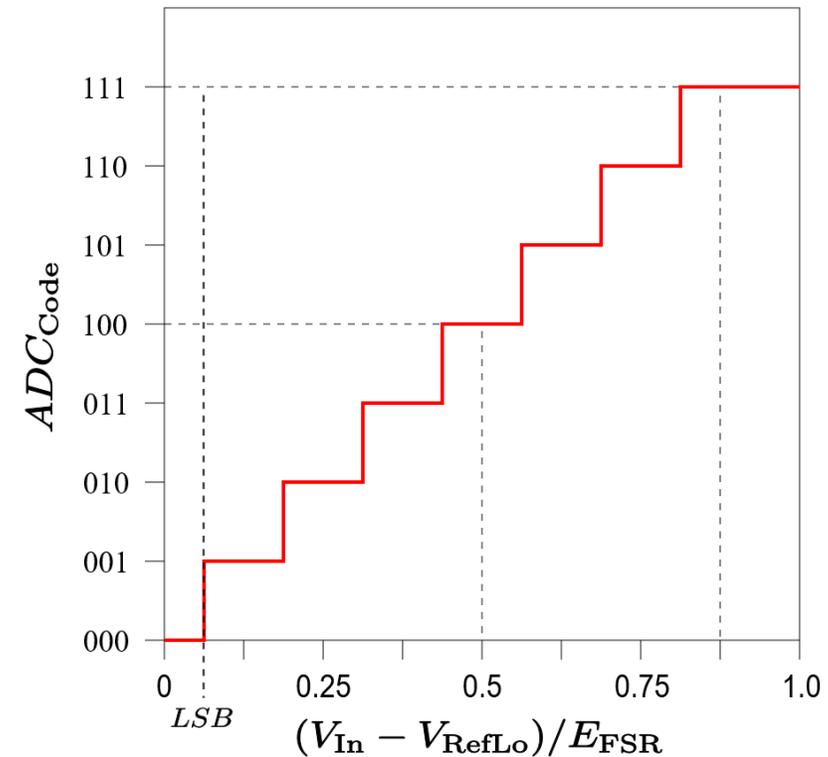
Source: [1]

[1] <http://spectrum.ieee.org/computing/hardware/moores-law-meets-its-match>



Analog to Digital Converters (ADC) Basics

- The most conceptually simple ADC is the N-bit ADC. It maps a set voltage level to a specific output.
- Another very common form of ADC is the $\Sigma\Delta$ ADC. It is beyond the scope of this talk, however, lots of great resources online [2]

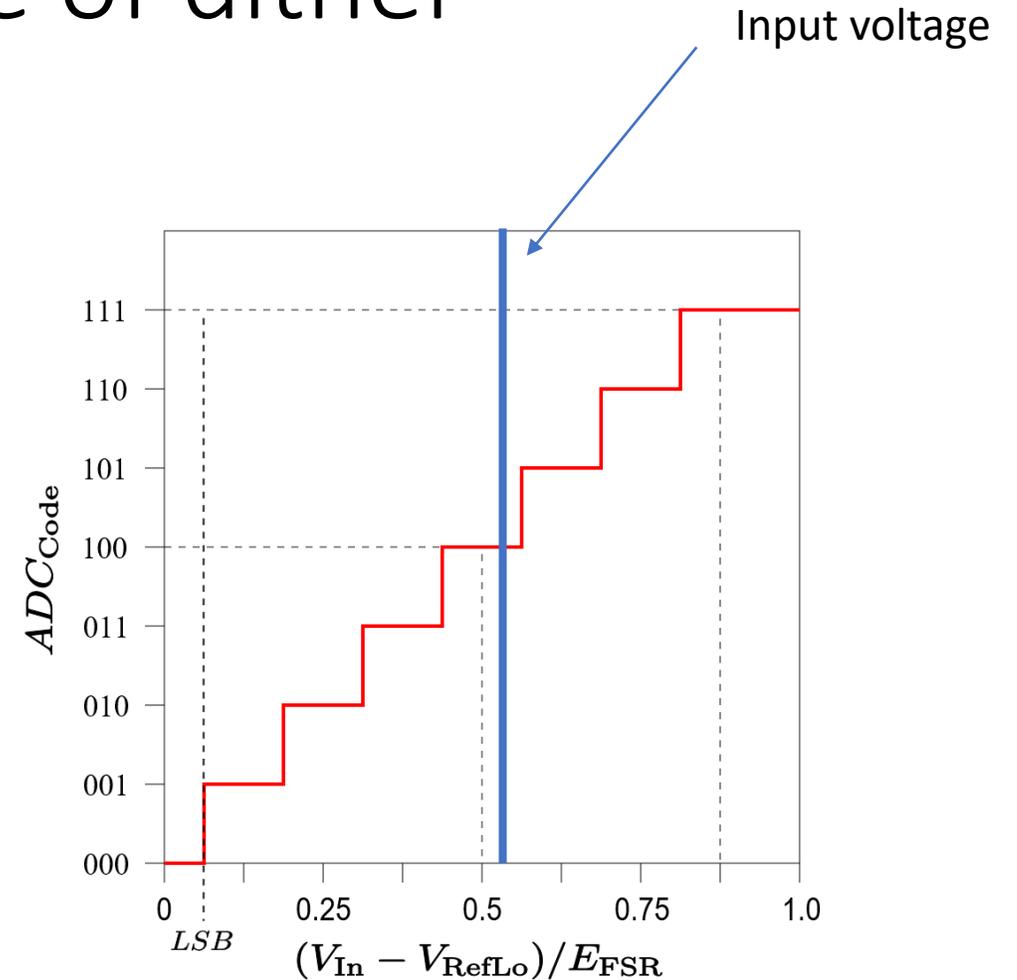


[1] Source: https://en.wikipedia.org/wiki/File:ADC_voltage_resolution.svg

[2] <https://www.maximintegrated.com/en/app-notes/index.mvp/id/1870>

ADCs and the importance of dither

- What if I feed an ideal 3-bit ADC a constant $0.51 \cdot V_{ref}$ input?
 - The output will *always* be 100, and this will be mapped to $0.5 \cdot V_{ref}$
- But what if I feed in: $0.51 \cdot V_{ref} +$ gaussian noise with a variance of $\Delta/2$?



Mapping ADC bits to SNR

$$\text{DR (dB)} = 6.021N + 1.761 \text{ (ideal N-bit ADC)}$$

=> direct result from examining quantization noise

$$\text{DR (dB)} = 6.021N - 4.260 \text{ (optimally-dithered N-bit ADC)}$$

Source: Course Notes, UT Austin EE382M-19: Mixed Signal System Design and Modeling, Eric Swanson



Analog to Digital Converters (ADC)

- ADCs have been improving at a rate that is analogous to Moore's Law
- Several Figures of Merit (FOM) have been defined that are useful in examining this performance growth
- **(Very) Roughly: 2dB/year improvement in dynamic range (>1MHz)**
 - Rate highly depends on sampling frequency
- Several Excellent Survey's exist:
 - Walden, Robert H. "Analog-to-digital converter survey and analysis." *IEEE Journal on selected areas in communications* 17.4 (1999): 539-550.
 - A/D-converter performance evolution (2012) [Online]. Available: <https://converterpassion.files.wordpress.com/2013/01/adc-performance-evolution-1v1.pdf>
 - B. Murmann, "ADC Performance Survey 1997-2016," [Online]. Available: <http://web.stanford.edu/~murmann/adcsurvey.html>.



ADC Performance Versus Time

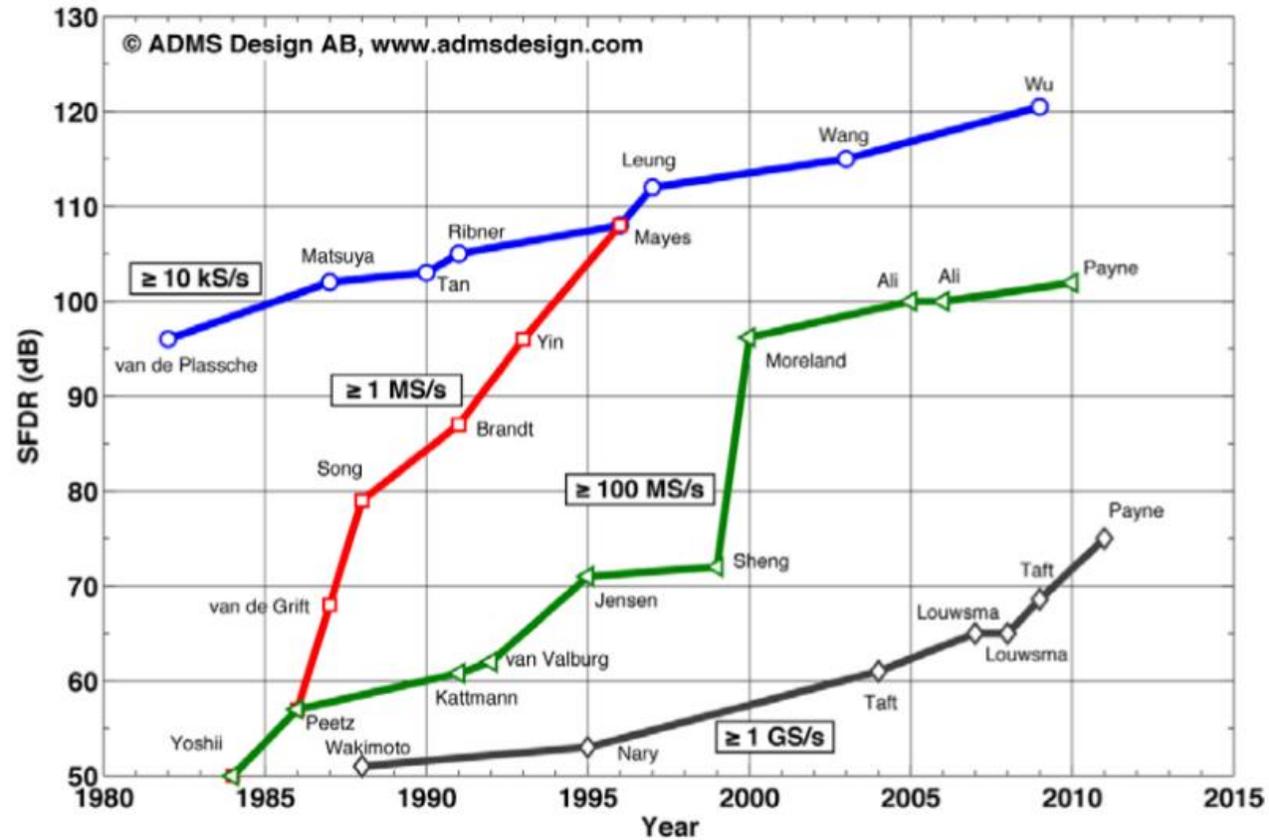


Figure 8.3. Scientifically reported ADC implementations: Peak SFDR evolution over time for minimum sampling rates of 10k (○), 1M (□), 100M (◁), and 1GS/s (◇).

Source: <https://converterpassion.files.wordpress.com/2013/01/adc-performance-evolution-1v1.pdf>



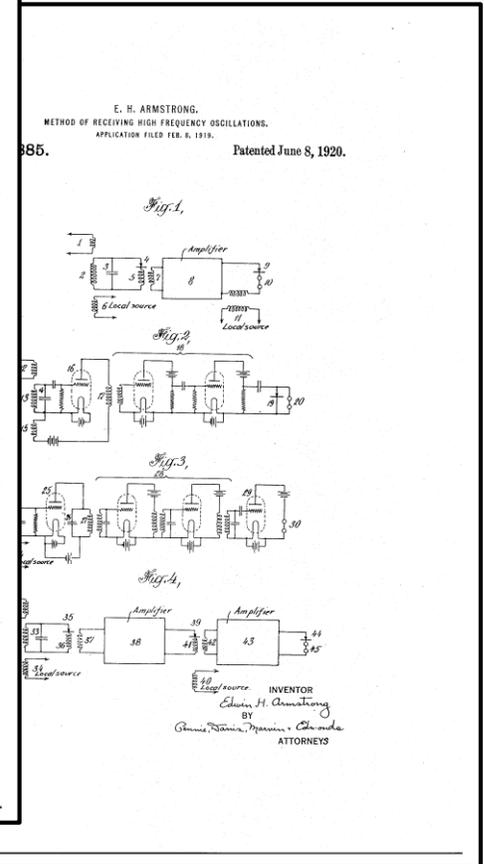
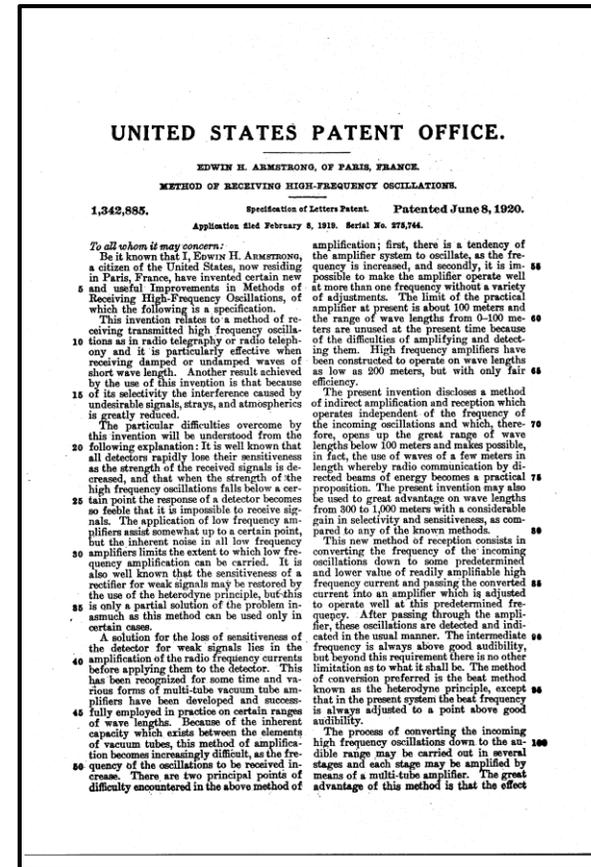
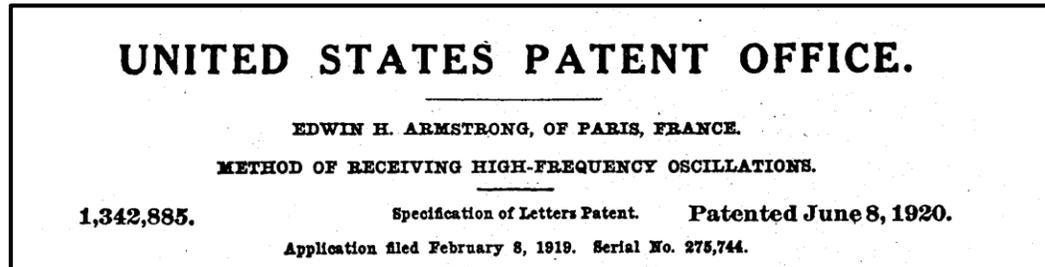
Traditional & Software Defined Radios



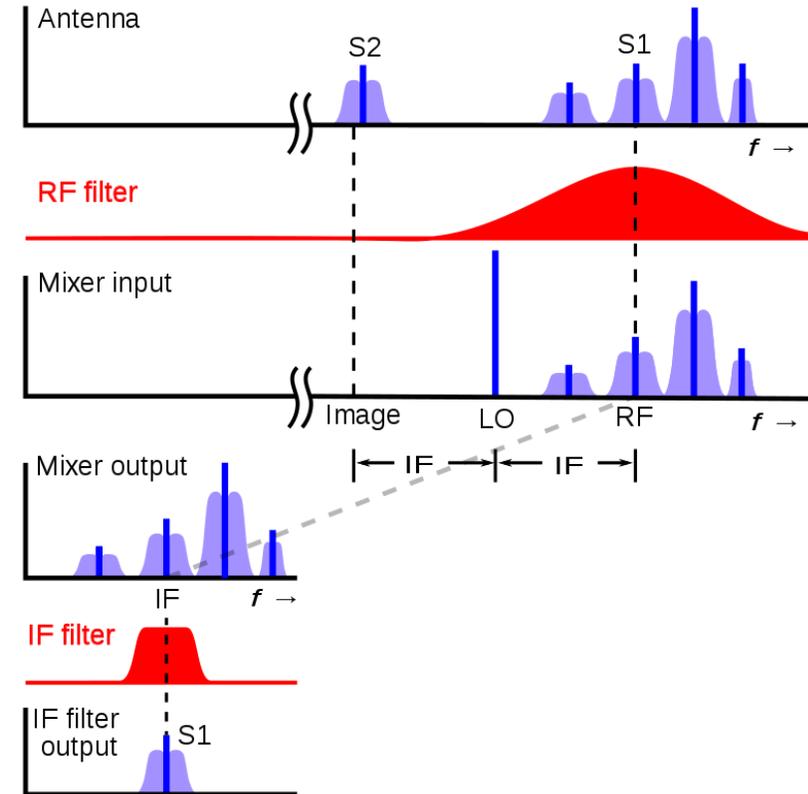
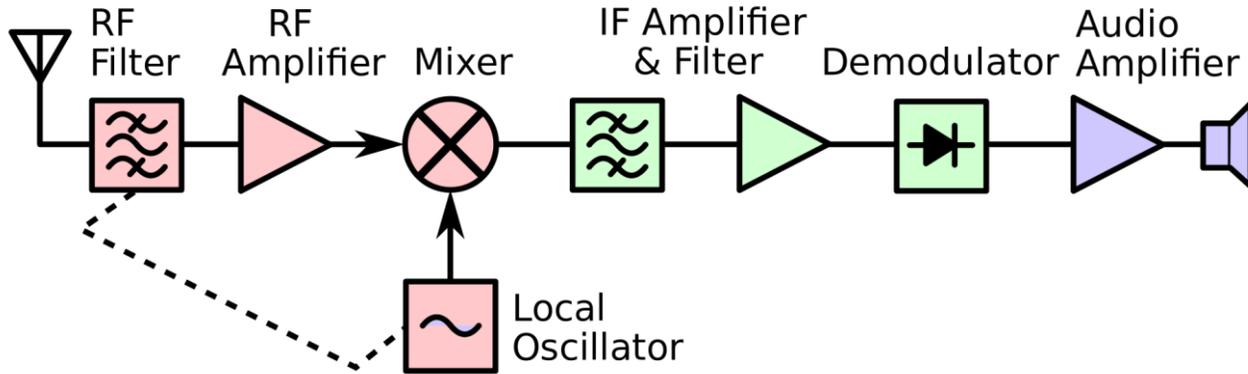
Superheterodyne receiver

- Armstrong's invention is one of the most important of the 20th century:

"Method of receiving high-frequency oscillations." U.S. Patent 1,342,885, issued June 8, 1920.



Superheterodyne receiver



Sources:

https://en.wikipedia.org/wiki/Superheterodyne_receiver#/media/File:Superheterodyne_receiver_block_diagram_2.svg

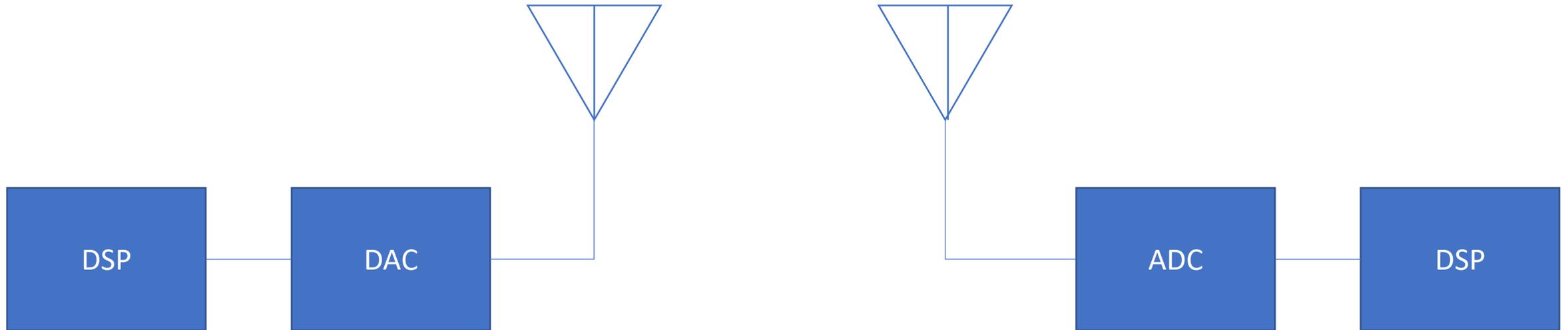
https://en.wikipedia.org/wiki/Superheterodyne_receiver#/media/File:How_superheterodyne_receiver_works.svg



But... we don't need that
anymore, we have SDR!

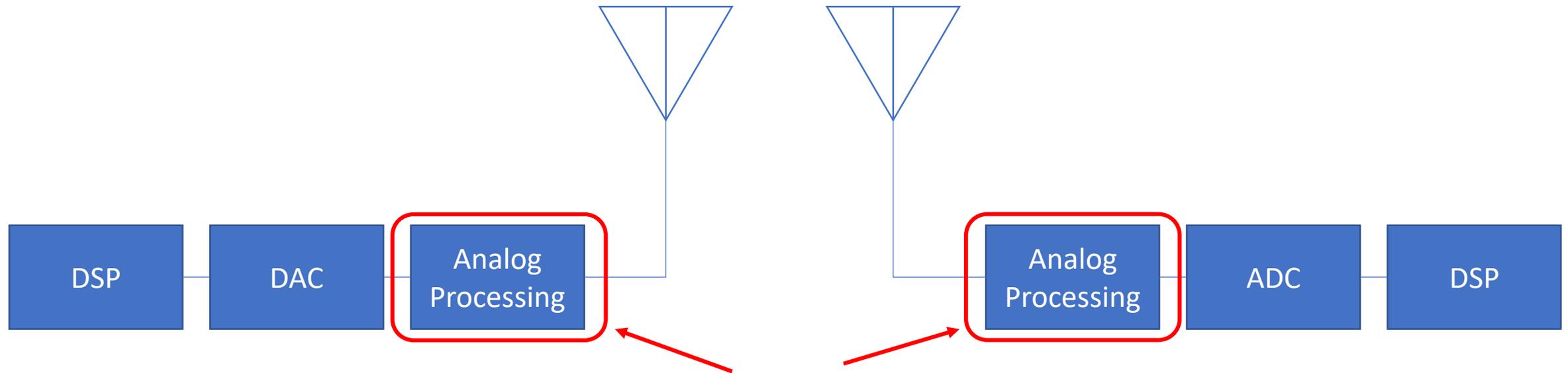


Conceptual SDR models: perception



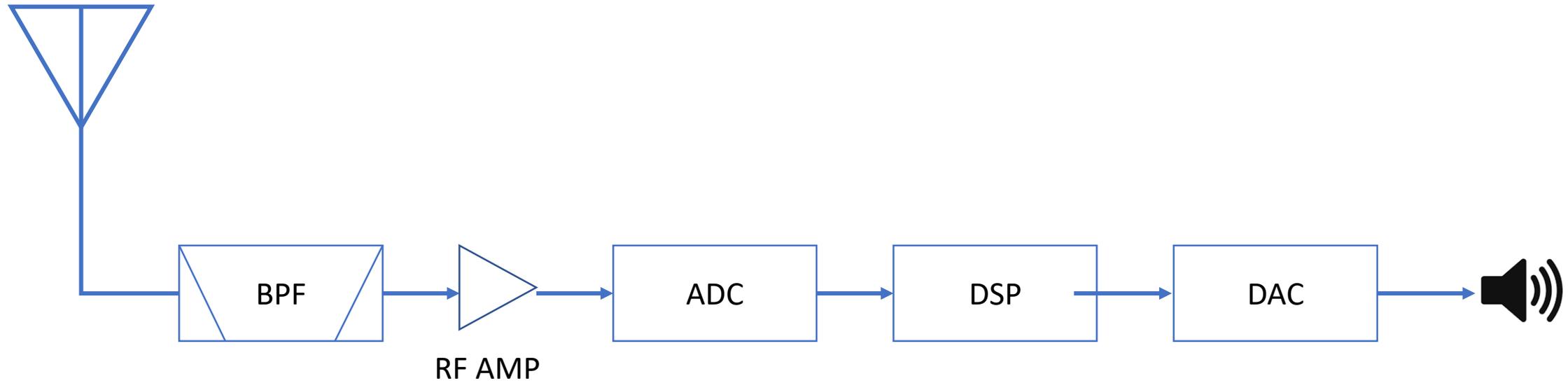
A common (and incorrect) model of software defined radios.
An ADC and an antenna, all we need?

Conceptual SDR models: reality

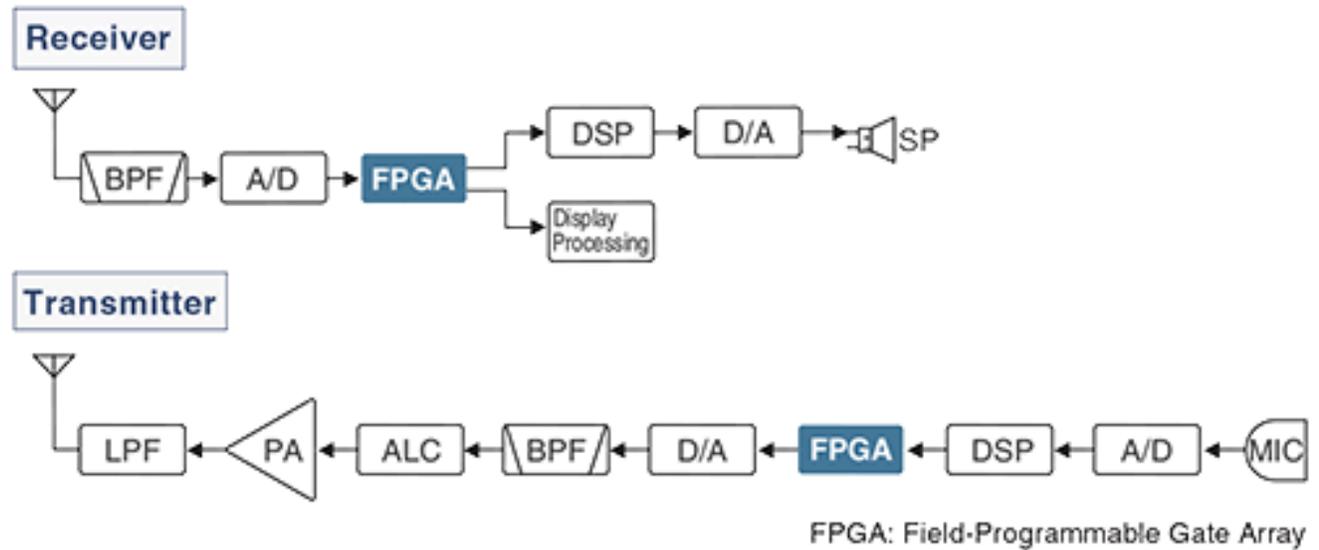


The analog processing can easily be as sophisticated and specialized to a particular frequency / bandwidth as a traditional transceiver design

Conceptual SDR models: Direct Sampling

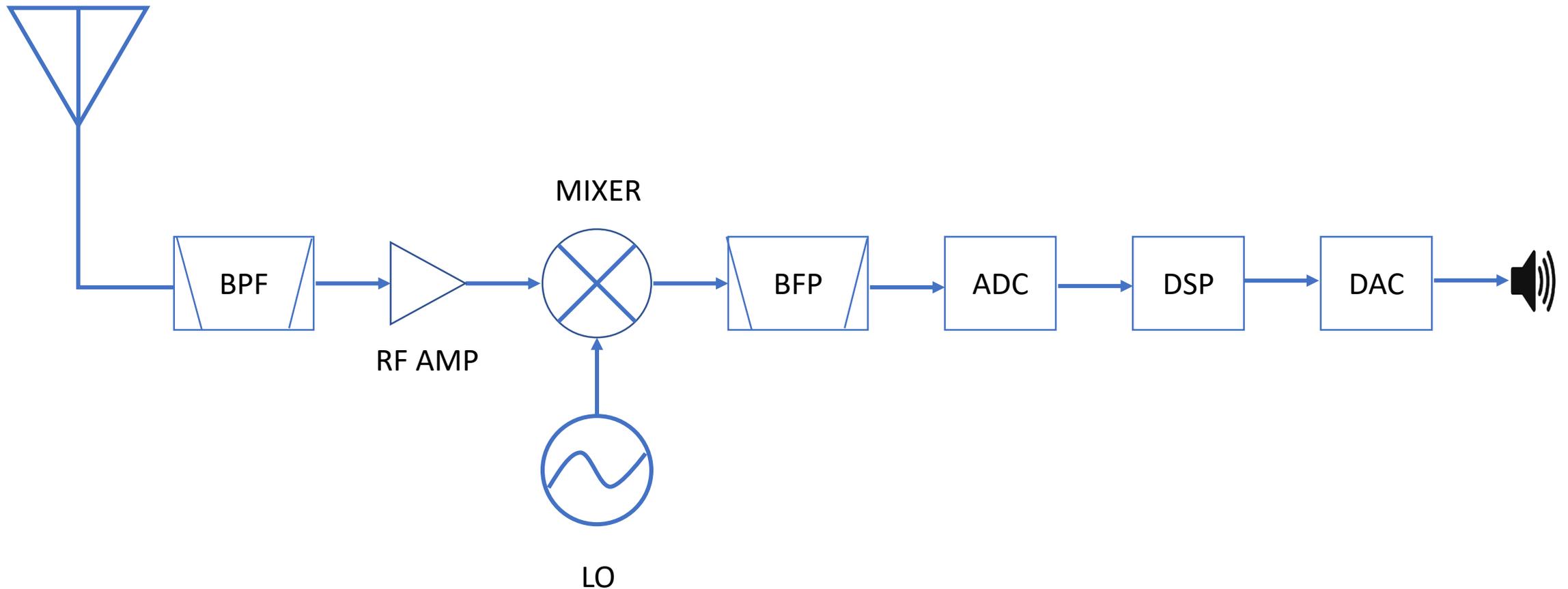


Commercial Example: IC-7300



Source: <http://www.icomamerica.com/en/products/amateur/hf/7300/default.aspx>

Conceptual SDR models: Superhet

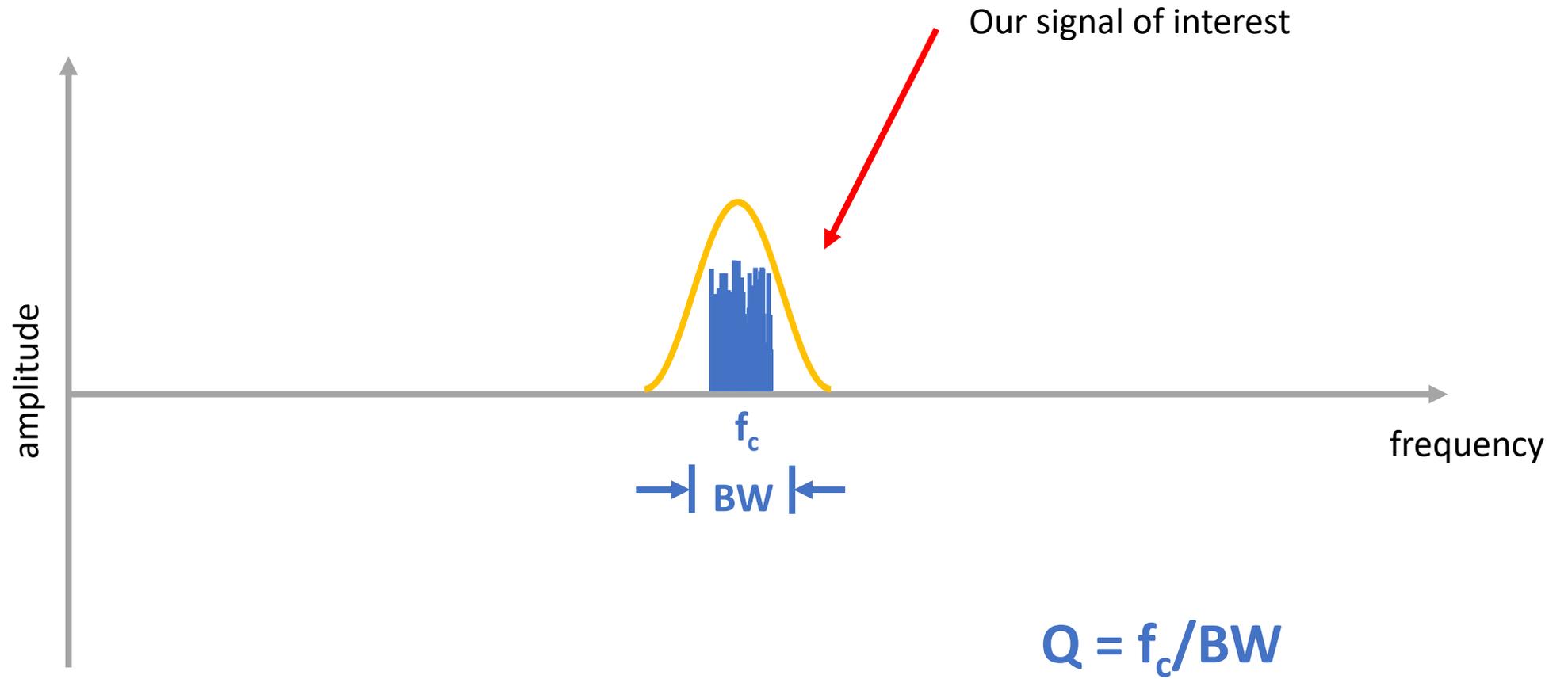


Analog design and SDRs

- Analog components of SDR are as important as the digital
 - Once undesired signals (noise, interference) are aliased into our desired signals there is no way to completely remove them
 - Antenna and front-end design are critically important
 - Proper analog filtering is very important
 - Practical amateur VHF+ designs will most likely *not* be directly sampled – they will use a mixer and an IF frequency
- Your antenna is an important part of the analog front-end
 - Antennas provide spatial and frequency selectivity



Filtering quality (Q) factor



What do we need for amateur VHF+ applications?

Band	Frequency (MHz)	Bandwidth (kHz)	Q Factor **
6 Meters	50.1 – 54.0	25	2000
2 Meters	144.1 – 148.0	25	5760
1.25 Meters	220.0 – 225.0	100	2200
70 cm	420.0 – 450.0	6000	70
33 cm	902.0 – 928.0	6000	150
23 cm	1240 – 1300	6000	207
13 cm	2300 – 2310	1000	2300
13 cm	2390 – 2450	1000	2390
9 cm	3300 – 3500	22000	150
5 cm	5650 – 5925	≥ 1000	5650
3 cm	10000 – 10500	≥ 1000	10000

** best case, e.g., highest bandwidth on ARRL bandplan

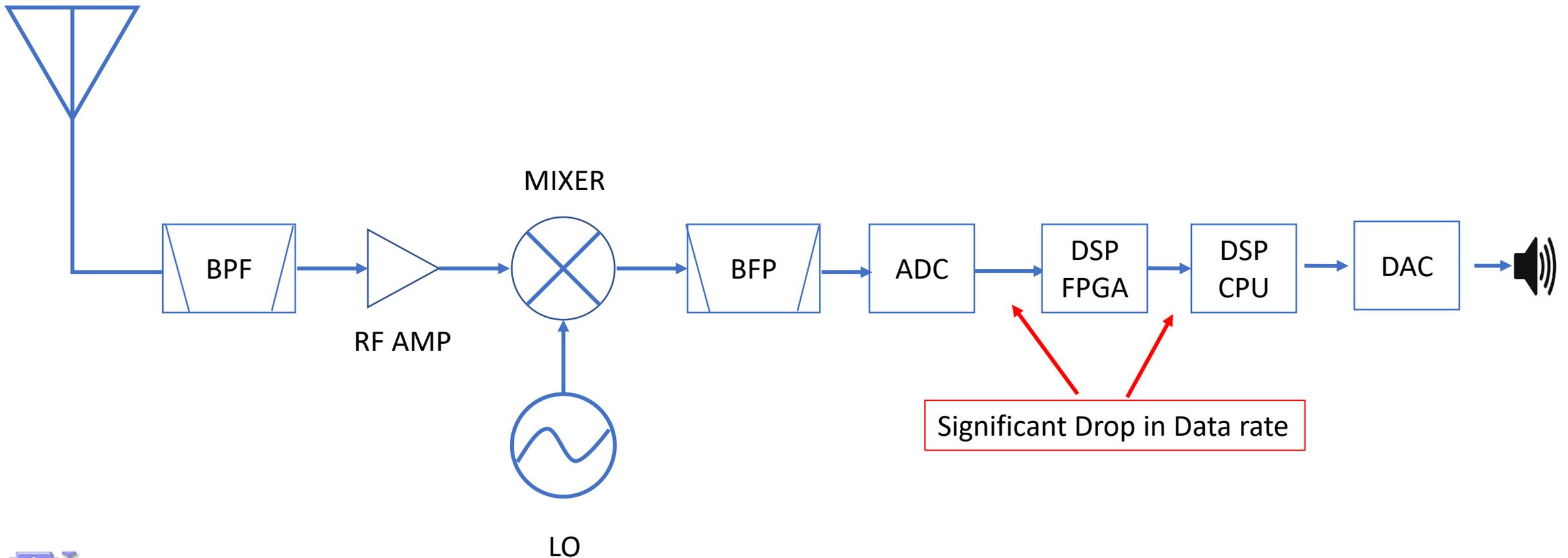


Those Q factors look awfully high...

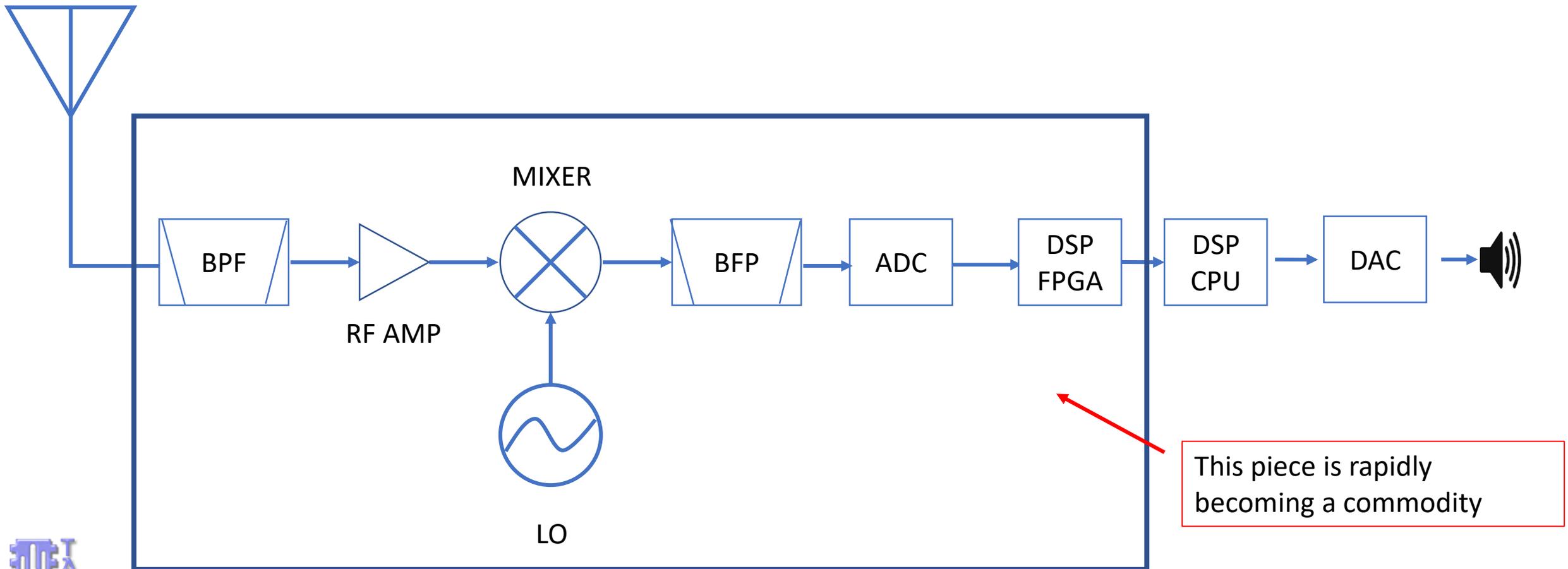
- In traditional analog designs these might require double or triple conversion...
- But no problem, we can get super high rate ADCs!
- Use a lower Q factor analog filter and then a brick wall (or cascading brick wall) FIR filter once the data is digitized.
- But wait... isn't that an awful lot of data?
 - Yes, more than we can deal with on a commodity PC / standard computer buses



Conceptual SDR models: With Pre-processing FPGA



Conceptual SDR models: With Pre-processing FPGA



Thick Pipe vs. Thin Pipe



Signal Processing

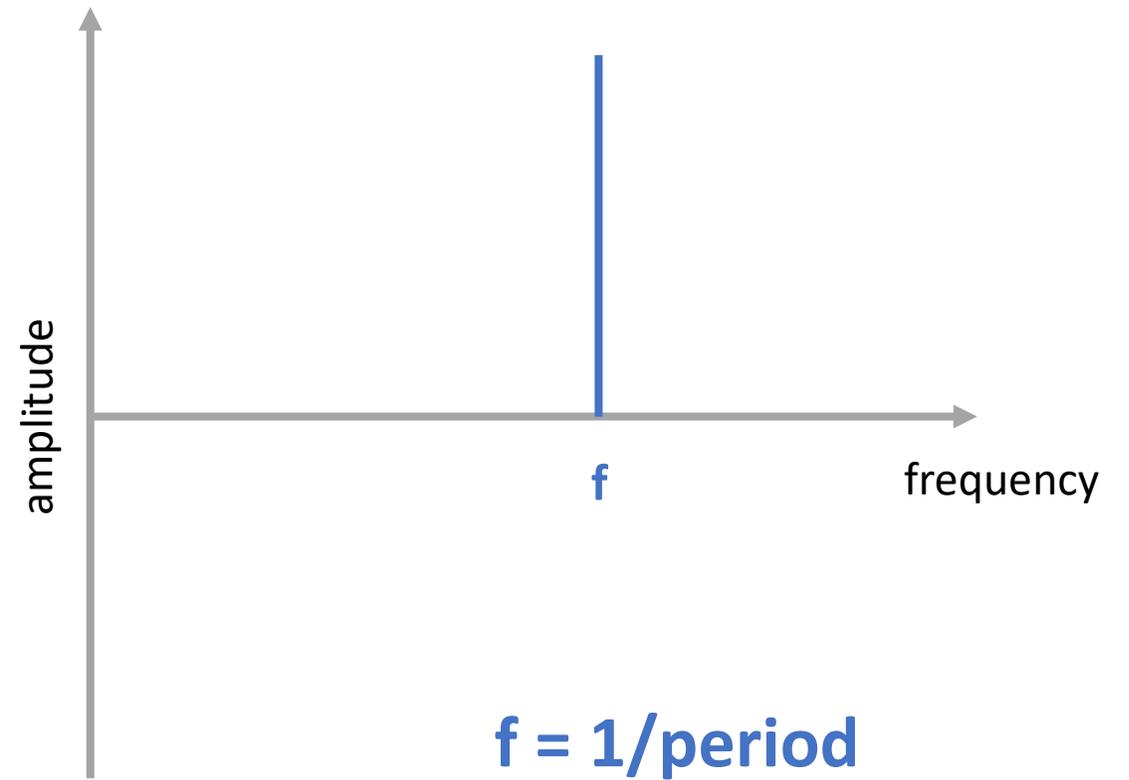
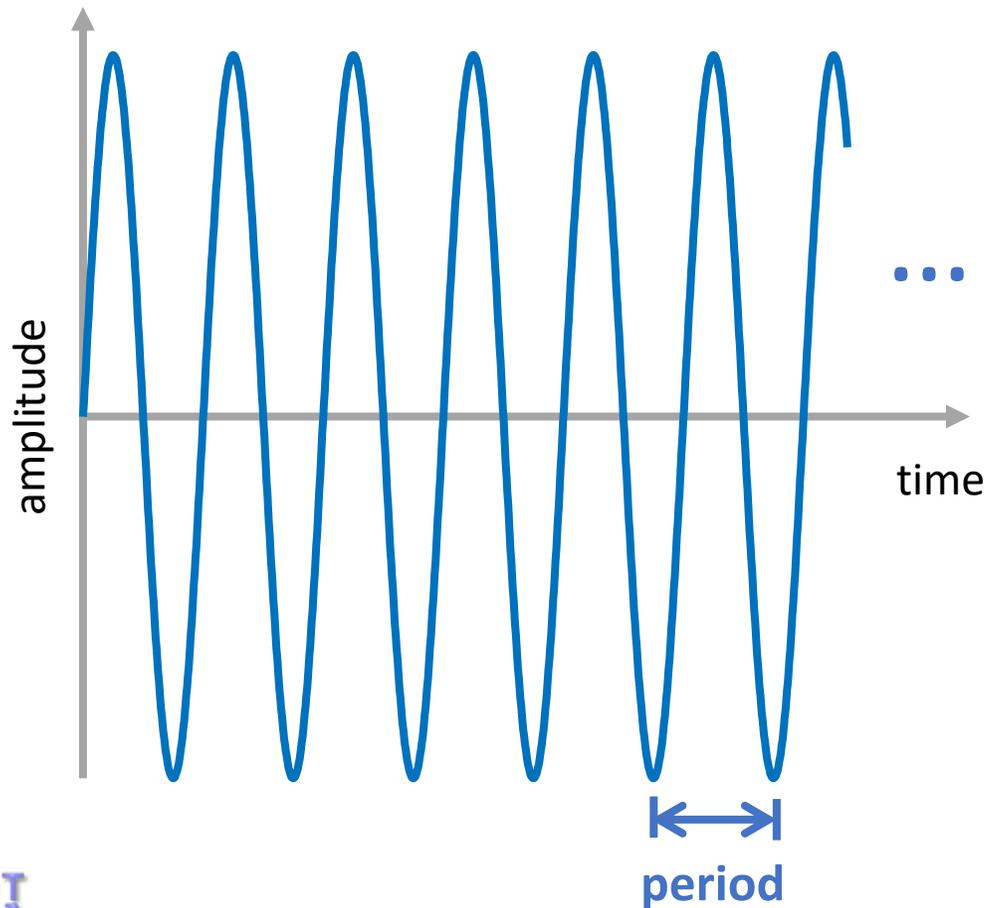


What is Signal Processing?

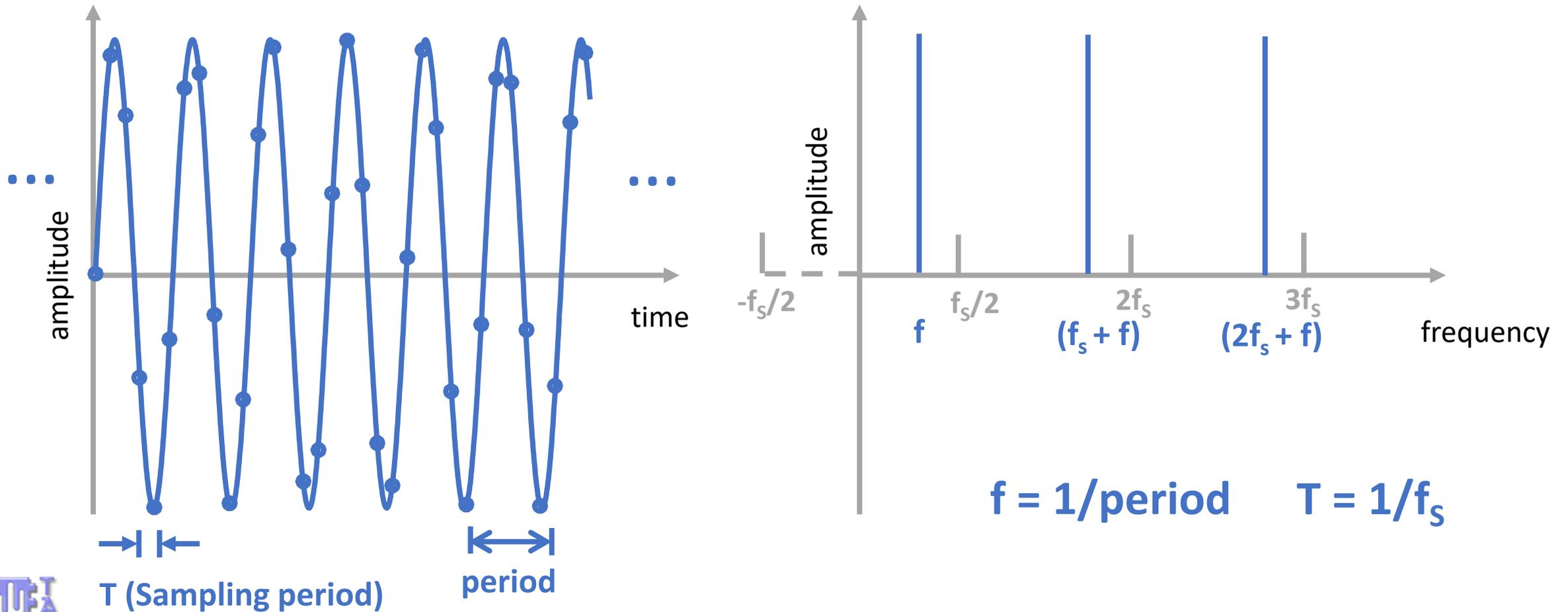
- Manipulation of signals representing real-world values such as amplitude, phase, temperature, etc.
- This manipulation of signals enhances them in some way:
 - Remove or lessen noise and interference
 - Accentuate a signal or signal attribute of interest
 - Extract information (e.g., demodulate digital information)
- Common signal processing tasks:
 - Filtering (attenuation of signals based on frequency)
- Typically involves working with both a time (continuous or discretely-sampled) and frequency (continuous or discretely-sampled) domain



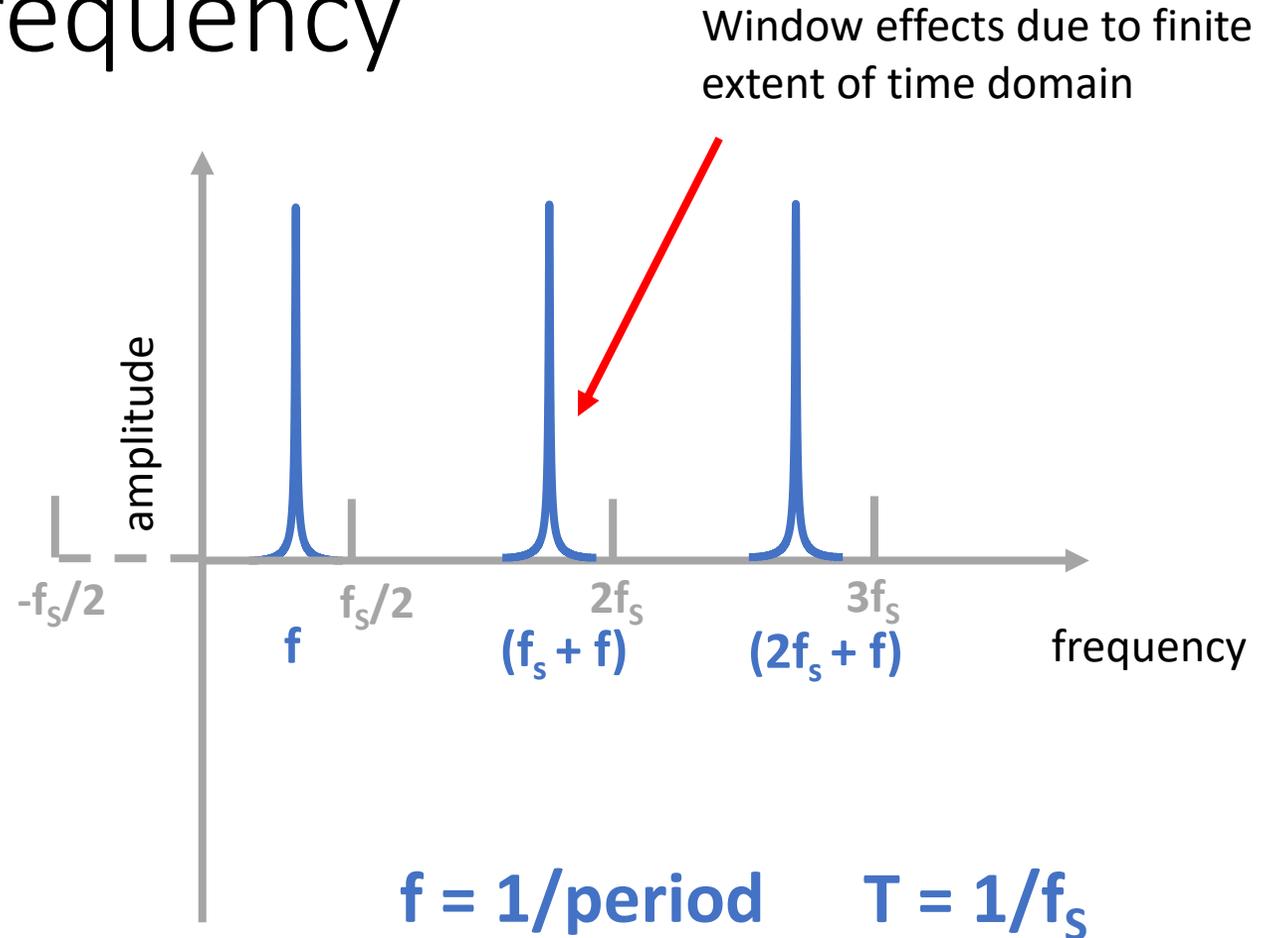
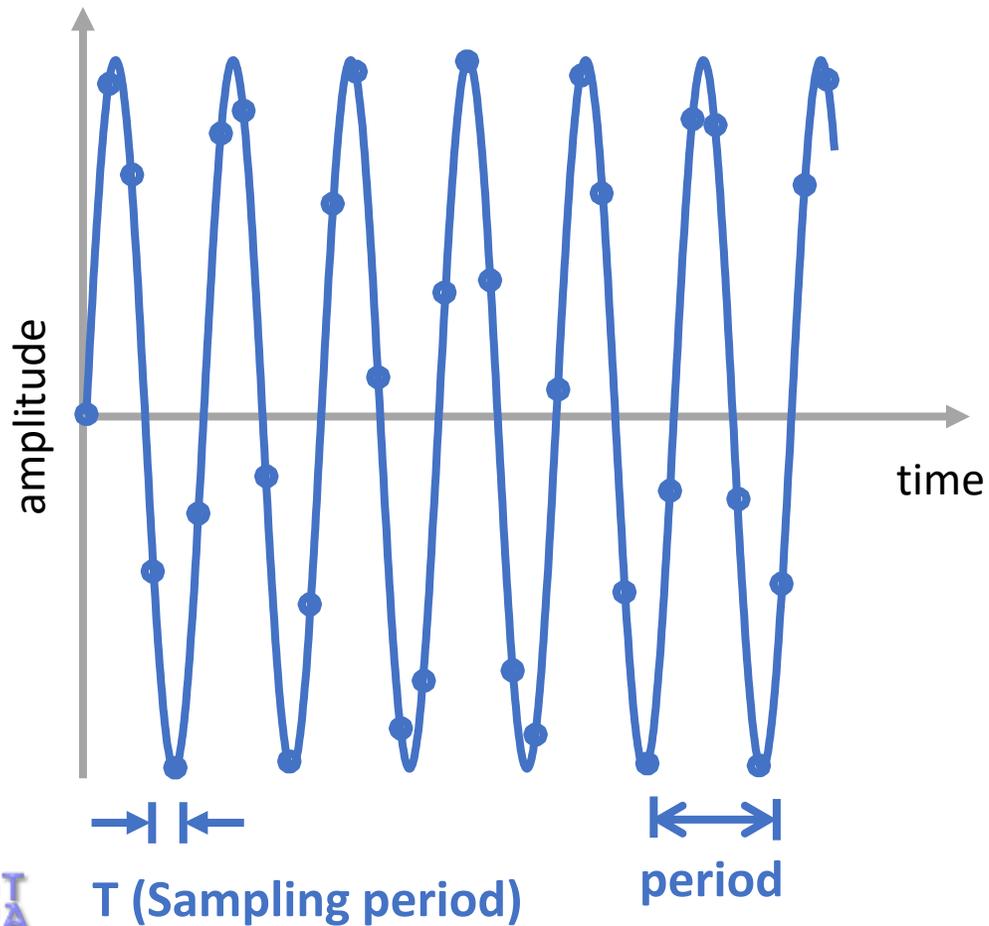
Time and Frequency Domains: Continuous



Time and Frequency Domains: Discrete Time



Time and Frequency Domains: Discrete Time and Frequency



Sampling

- Sampling in one domain leads to periodicity in the other
- **Nyquist–Shannon sampling theorem [1]**
 - “If a function $x(t)$ contains no frequencies higher than B hertz, it is completely determined by giving its ordinates at a series of points spaced $1/(2B)$ seconds apart.”
- Anything outside the frequency limits will alias

[1] Shannon, Claude Elwood. "Communication in the presence of noise." *Proceedings of the IRE* 37.1 (1949): 10-21.



Signal Processing Domains for Mixed-signal Systems

Type of Signals	Time	Frequency	Fourier Transform	Filter Design
Continuous time analog processing	Continuous	Continuous	Continuous Fourier Transform	Laplace Transform (s-domain)
Sampled-data analog processing	Discrete	Continuous (Periodic)	Discrete-time Fourier Transform (DTFT)	Z-Transform (z-domain) **
Sampled-data digital Processing	Discrete (Periodic)	Discrete (Periodic)	Discrete Fourier Transform (DFT)	Z-Transform (z-domain) ** / DFT

**For IIR Filter Design we can use the bilinear transform $s = \frac{2(z-1)}{T(z+1)}$



Analog processing

- Mixed-signal design (that is, analog and digital on one chip) is very difficult
 - Only a handful of development group capable of achieving world class performance
- Component variations huge compared to discrete analog
- Component aging also a big concern
- A successful design will likely utilize external analog filtering
- Suggestions for designing analog filters:
 - The theory and math behind filter design is fairly accessible
 - No need to use canned design tools, dig into the design!
 - Analog filter design is typically taught in a EE course titled “Circuit Design” with lots of material available on the open web
 - Learn the basics of the Laplace transform
 - Sanity check and DC and Daylight
 - Use consistent axis when plotting responses to build intuition



Resources for further Learning

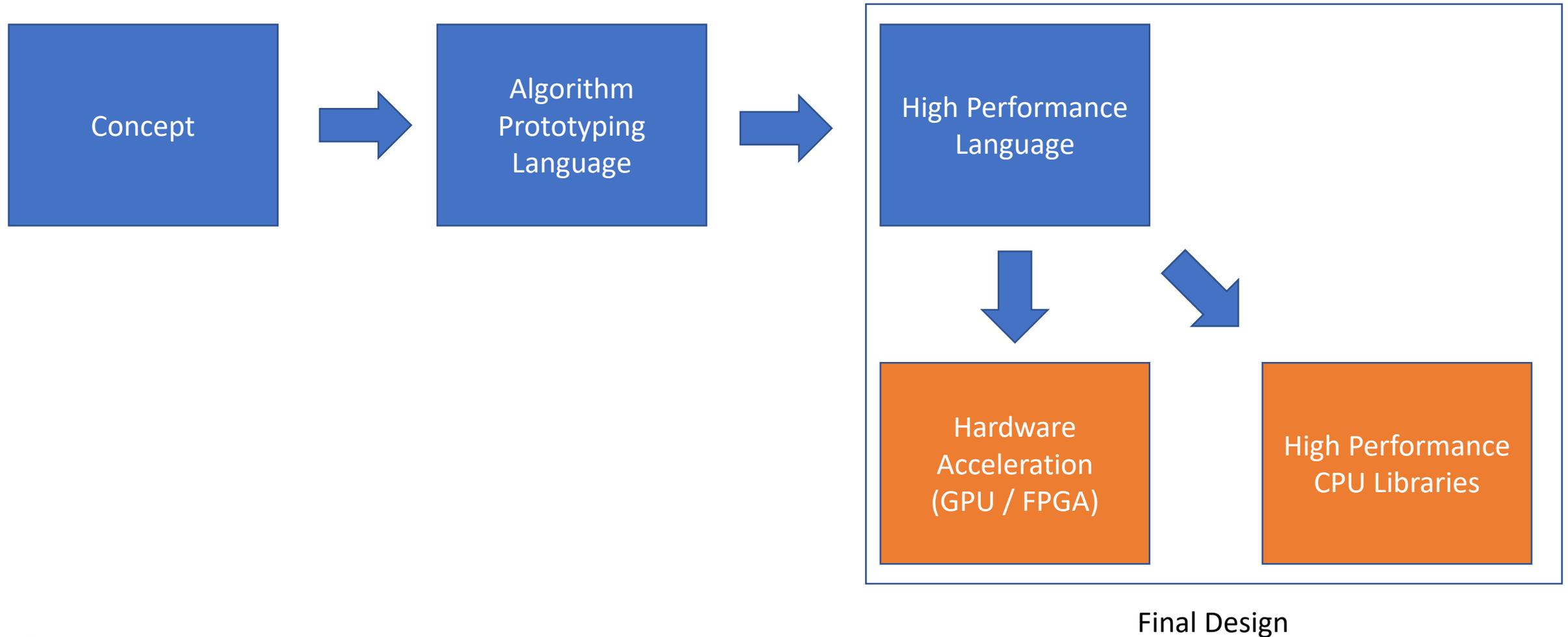
- MIT Open Courseware: Digital Signal Processing
 - Prof. Alan V. Oppenheim
 - <https://ocw.mit.edu/resources/res-6-008-digital-signal-processing-spring-2011/video-lectures/lecture-14-design-of-iir-digital-filters-part-1/>
- Analog Filter Design (e.g., Laplace Transforms)
 - Typically covered in an undergrad course called Electric Circuits
 - <https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-002-circuits-and-electronics-spring-2007/index.htm>
 - Also covered in Digital Signal Processing (DSP) Courses (e.g., Lecture 14 in MIT course)
 - Lots of HAM recourses
 - For example: <http://www.arrl.org/rf-and-af-filters>
- Digital Filter Design
 - Covered in DSP Courses (e.g., Lecture 17 in MIT Course)



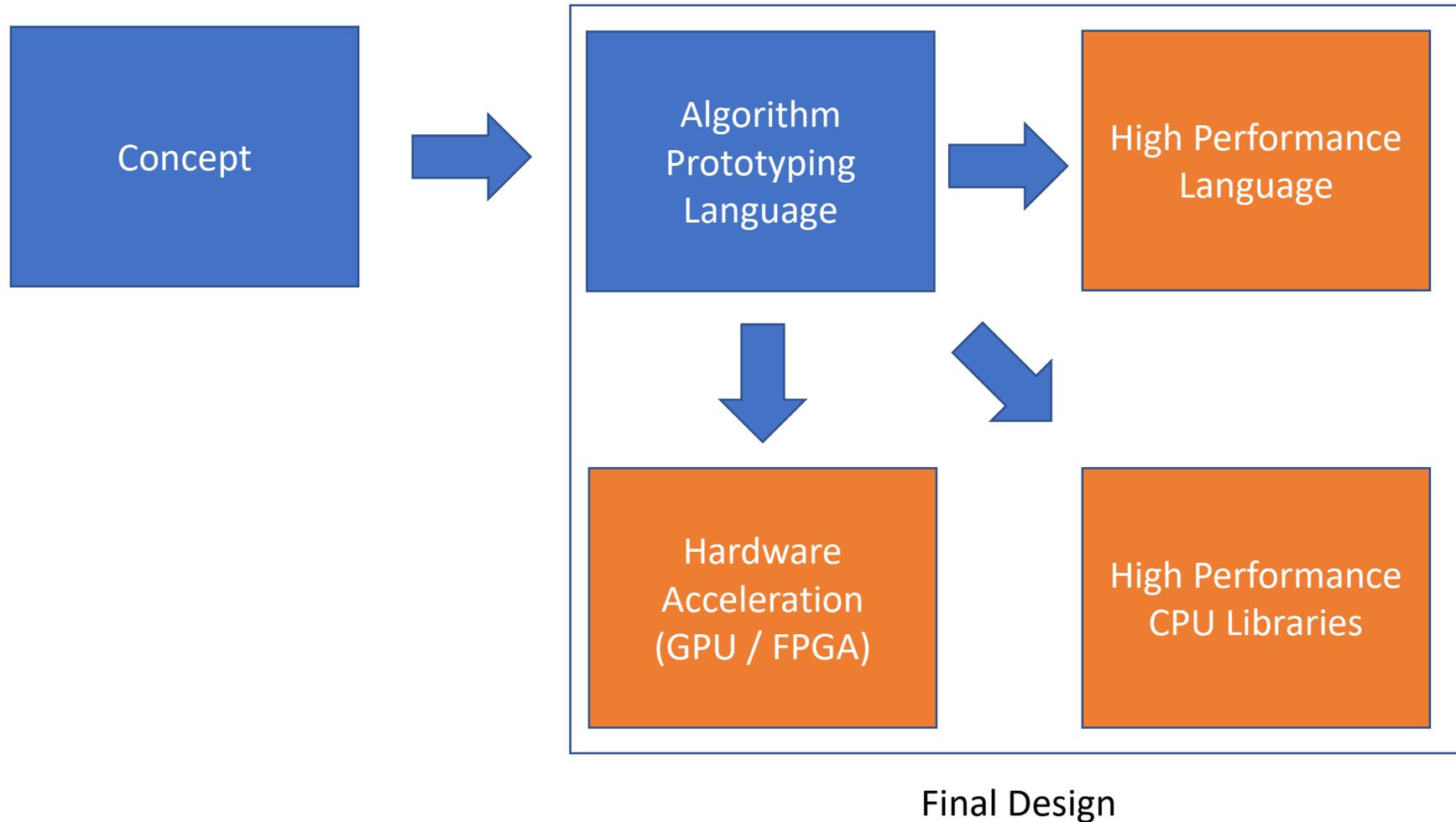
Practical DSP: Theory and Implementation



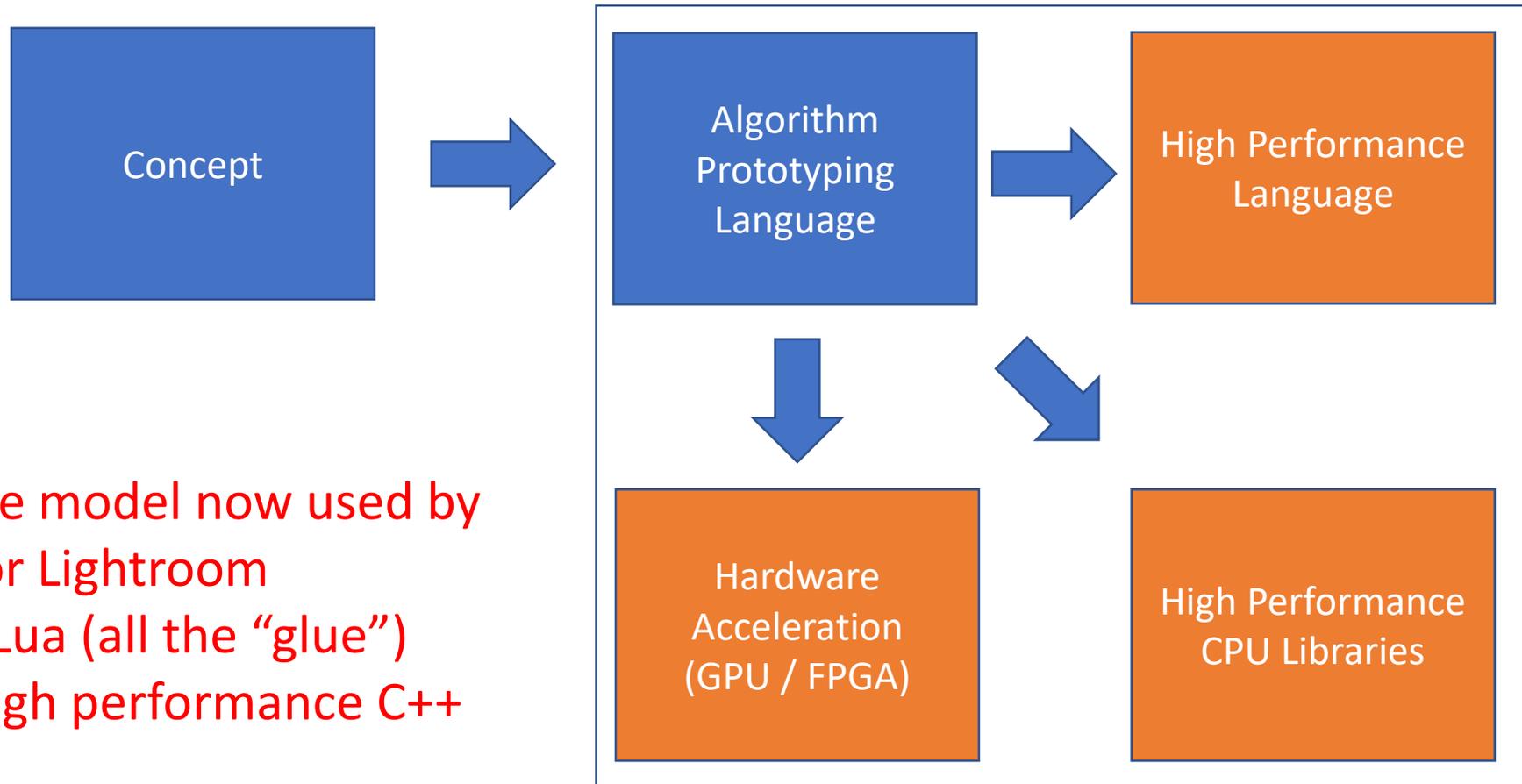
Signal Processing Development Model (1)



Signal Processing Development Model (2)



Signal Processing Development Model (2)



This is the model now used by Adobe for Lightroom

- 60%+ Lua (all the “glue”)
- 30% high performance C++



Development Environments

- Algorithm development / prototyping languages
 - MATLAB (Octave / Scilab)
 - Scientific Python
 - Julia
- High performance languages and libraries
 - C/C++
 - Classic Numerical Libraries (BLAS, LAPACK)
 - OpenMP, OpenCL, CUDA
 - C++ Templated Libraries
 - Armadillo, Eigen, FLAME
- Hardware Acceleration
 - VHDL
 - OpenCL (High level language that supports GPU / FPGA acceleration)



MATLAB

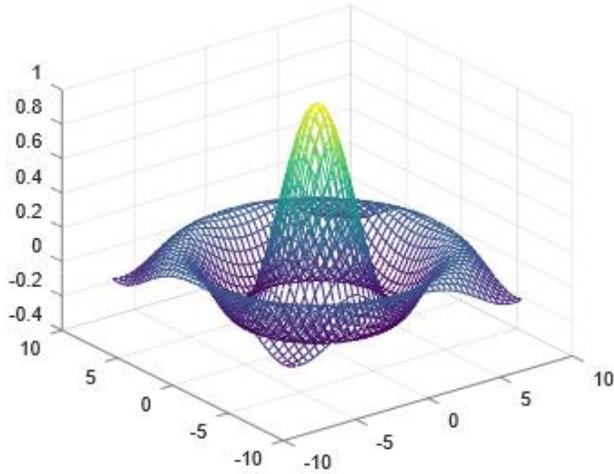
- The defacto (and in my opinion, best) algorithm design language for signal processing
- Expensive for commercial use, but relatively inexpensive for personal, hobby, and student licenses
- Home: \$149 Base + \$49 / add on
- Student: \$49 Base + \$29 / add on
- Great debugger and visualization support build in
- Used in many classrooms, and so there is a lot of support on the web
- **Born in New Mexico! (Clive Moler / UNM)**



<http://mathworks.com>



MATLAB compatible languages



GNU Octave

<http://gnu.org/software/octave>



Scilab

<http://scilab.org>

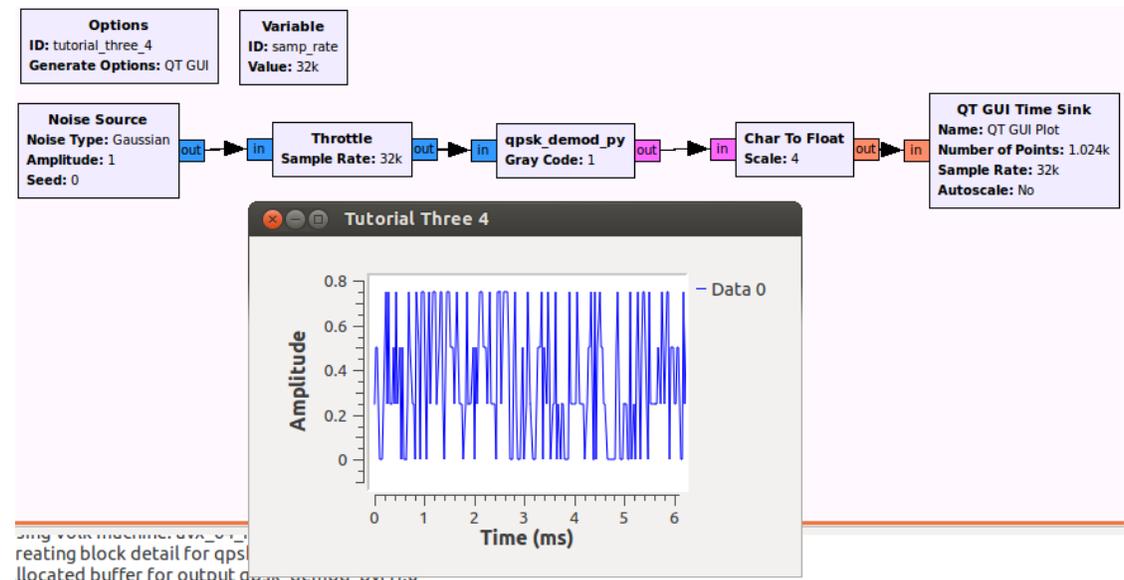


FreeMAT

<http://freemat.sourceforge.net/>

GNU Radio

- Free, open source
- Actively developed
- Lots of add on packages available
- Provides signal processing blocks that can be tied together to implement software radios

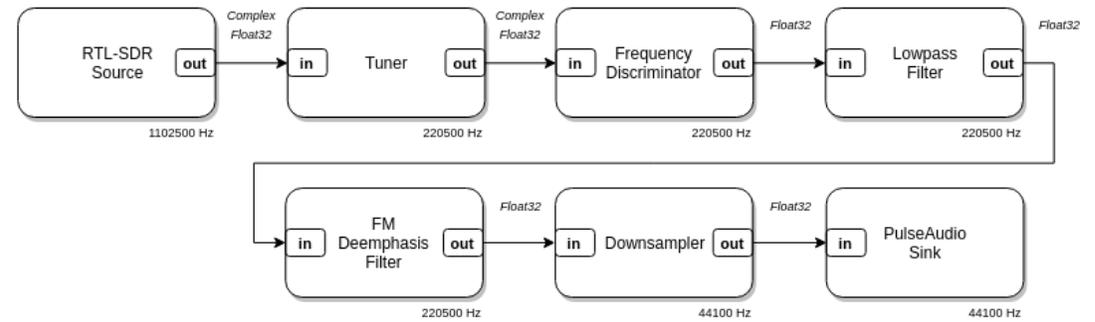


<http://gnuradio.org>



LuaRadio

- Free, open source
- Actively developed
- Lightweight, embeddable flow graph signal processing framework for software-defined radio.
- Similar to GNU Radio, but smaller and more lightweight: designed to be embedded



<http://luaradio.io/>



Scientific Python

- Free, open source
- Actively developed
- Lots of add on packages available
- Integrates well with compiled C/C++ code
- Actually refers to a set of base packages:
 - Python
 - NumPy
 - SciPy
 - Matplotlib
 - etc...
- Several different interfaces are available
 - iPython
 - Spyder
 - ...



<https://www.scipy.org/>

SciPy Distributions

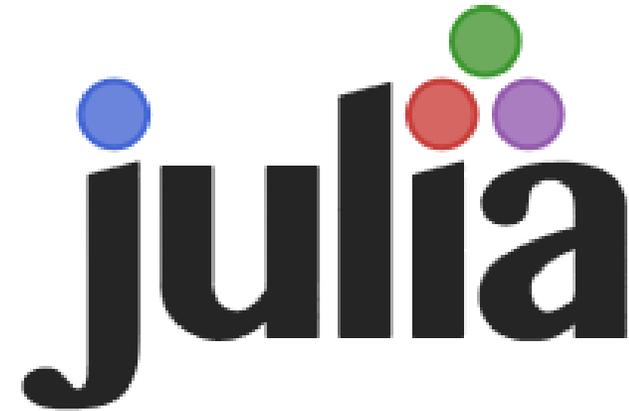
- Anaconda (<https://www.continuum.io/downloads>)
- Enthought Canopy (<https://www.enthought.com/products/canopy/>)
- Python(x,y) (<http://python-xy.github.io/>)
- WinPython (<http://winpython.github.io/>)
- Pyzo (<http://www.pyzo.org/>)

SciPy.org provides links to all of the above



Julia

- Free, open source
- Actively developed
- Lots of add on packages available
- Integrates well with compiled C/C++ code



<https://julialang.org/>

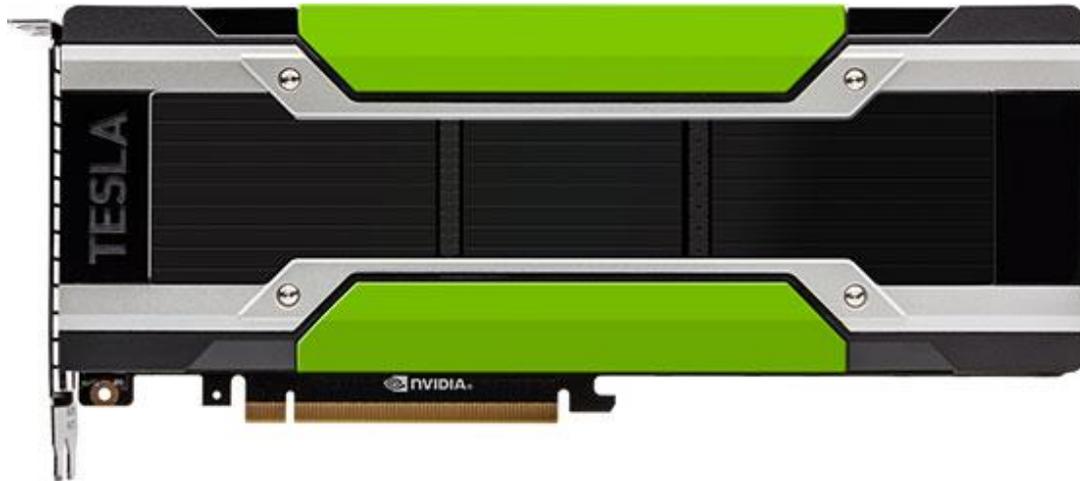
High performance numerical libraries

- First, the classics:
 - Basic Linear Algebra Subprograms (BLAS)
 - <http://www.netlib.org/blas/>
 - Linear Algebra Package (LAPACK)
 - <http://www.netlib.org/lapack/>
 - Fastest Fourier Transform in the West (FFTW)
 - <http://www.fftw.org>
- Templated Metaprogramming:
 - Armadillo: C++ Linear Algebra
 - <http://arma.sourceforge.net>
 - FLAME
 - <http://www.cs.utexas.edu/~flame/web/>
- Open Computing Language (OpenCL)
 - <https://www.khronos.org/opencvl>



Hardware Accelerators

GPUs



5.3 TeraFLOPS double / 10.6 TeraFLOPS single

NVIDIA Tesla P100

Source: <http://www.nvidia.com>

FPGAs



Two Arria 10 FPGAs / 3+ TeraFLOPS

Nallatech 510T

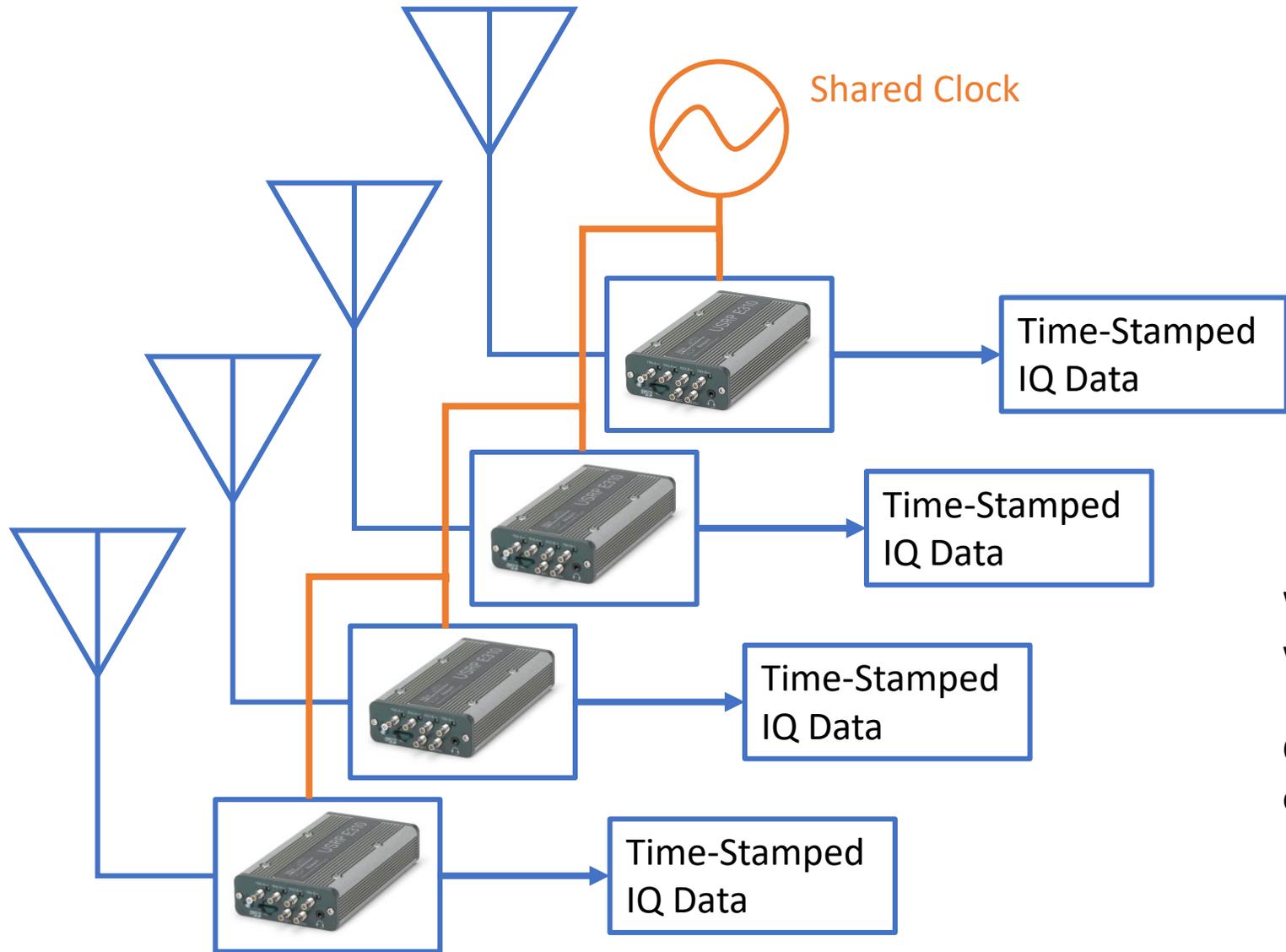
Source: <http://www.nallatech.com>



Ham Applications



Beamforming: Local

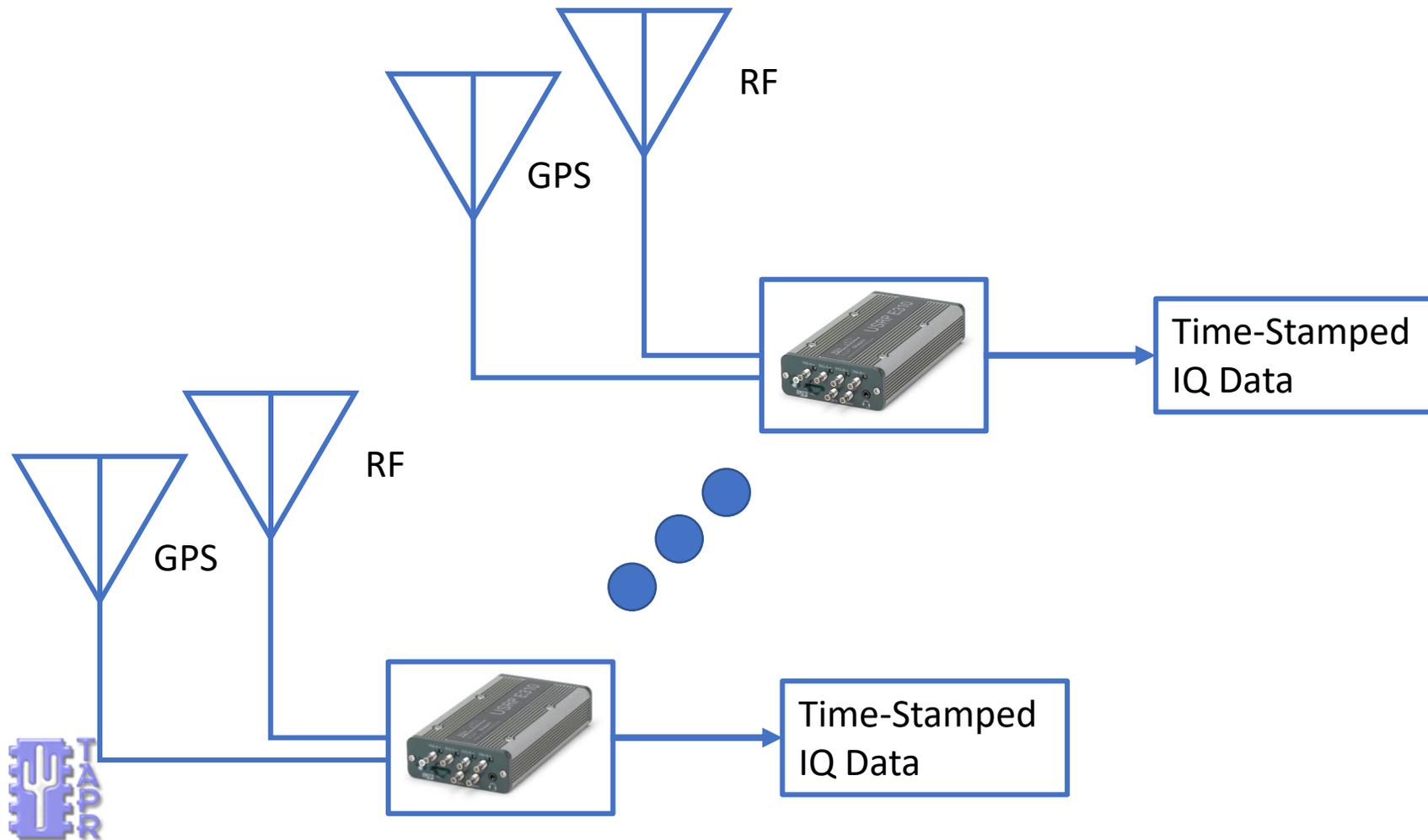


We can form any beam we want in post-processing!

Can also steer NULLS to notch out noise sources



Beamforming: Distributed



Could we build a large scale distributed receiver for HAM experimentation over the internet?

Hat Tip: Ed James KA8JMW

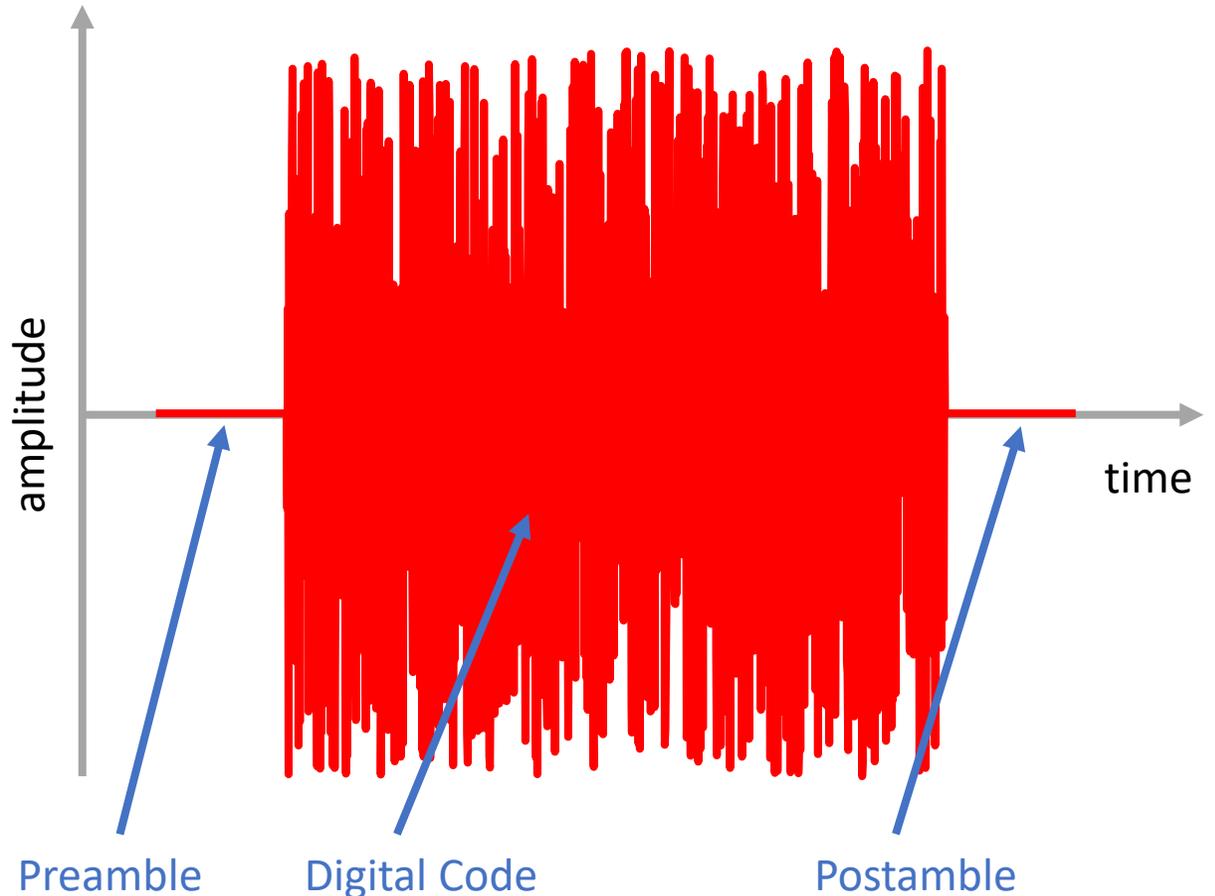
Beamforming: Distributed (Alternative)

- There are many commercial transmitters that have very good time stability
- For example: cell phone towers
- Can we have multiple digital receivers capture a known signal and cross correlate for timing?
 - For instance, the GSM Frequency Correction Channel (FCCH)



Beacon Concept

- Transmit a message consisting of:
 - Preamble
 - Message
 - Postamble
- Steer beam and run a search for preamble and postamble
 - Once detected can use to measure frequency drift
- Demod digital code for verification
- Total probability of false alarm is:
$$\text{PFA} = 1 - (1 - \text{PFA}_{\text{PRE}})(1 - \text{PFA}_{\text{CODE}})(1 - \text{PFA}_{\text{POST}})$$



Questions?

