

A Fast Switching, Wide Bandwidth Transceiver for 70-cm Operation, The DVR 4-2

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After designing, building, testing, beta testing, and finally shipping DVR 2-2 transceivers in early 1990, it became apparent quickly that there was a desire by many amateurs for an even faster transceiver for the 70-cm band. Features similar to those provided for by the DVR 2-2 were requested: fast TR switching, access to the modulator and discriminator without radio modification, data output independent of squelch, receiver derived carrier detection, simple design, and easy to work on. In addition, several suggested adding a filter for wide bandwidth operation, allowing for speeds higher than 9600 baud for networking (backbone) applications.

With these inputs in mind, the following broad specifications emerged for a simple straightforward 70-cm transceiver for 1200, 9600 and 19,200 baud operation:

- two bandwidth modes of operation, narrow and wide
- two receiver modes of operation, terrestrial and satellite (AFC)
- two data ports, one DVR 2-2 plug compatible, one for 19,200 operation, both without audio processing (no processing)
- TTL compatible signal levels for the 19,200 port, i.e. TTL ready
- fast TR switching
- a receiver derived carrier detect
- simple
- easy to work on
- easy to modify
- fun!

After considering a number of alternatives, regulatory requirements, and available ICs, we settled on a design represented in block

diagram form by Figures 1 and 2. The receiver again, like the DVR 2-2, is built around the Motorola 3362, but additional 'glue' was added. Second, in order to gain fast TR switching, the local oscillators for transmit and receive are crystal based, derived from a wide bandwidth phase locked loop consisting of a VCO, a divide by 64 counter, digital phase detector, wide loop filter and the crystal oscillators.

Block Diagrams

The receiver and transmitter portions of the unit, less local oscillator generation are denoted in Figure 1. LO generation, TNC interfacing ports, TR control and modulation/demodulation are represented in Figure 2. Let's start by considering the traditional transceiver section, Figure 1.

The receiver is triple-conversion and based on the Motorola 3362 'receiver on a chip,' with additions. The receiver chain, from reception to detector consists of (from left to right) receive PIN TR switch, RF preamplifier and first mixer, and the 3362 receiver on a chip with narrow and wide bandwidth filters for the third IF, 455 KHz. As with the DVR 2-2, the second IF is at 10.7 MHz, thereby using conventional, easily sourced parts. The transmitter is straightforward (from top right to left), consisting of VCO at frequency, an amplifier and PIN switch to provide for LO to both transmitter and receiver, and two stages of power amplification, followed by the transmit PIN switch at the antenna port.

Push-to-talk (PTT) via the mic input or from either data port controls the position of both the antenna and LO PIN switches. A front panel switch denoted by narrow/wide (N/W) determines which 455 KHz IF filter is

Figure 1 - DVR 4-2 Transmitter and Receiver

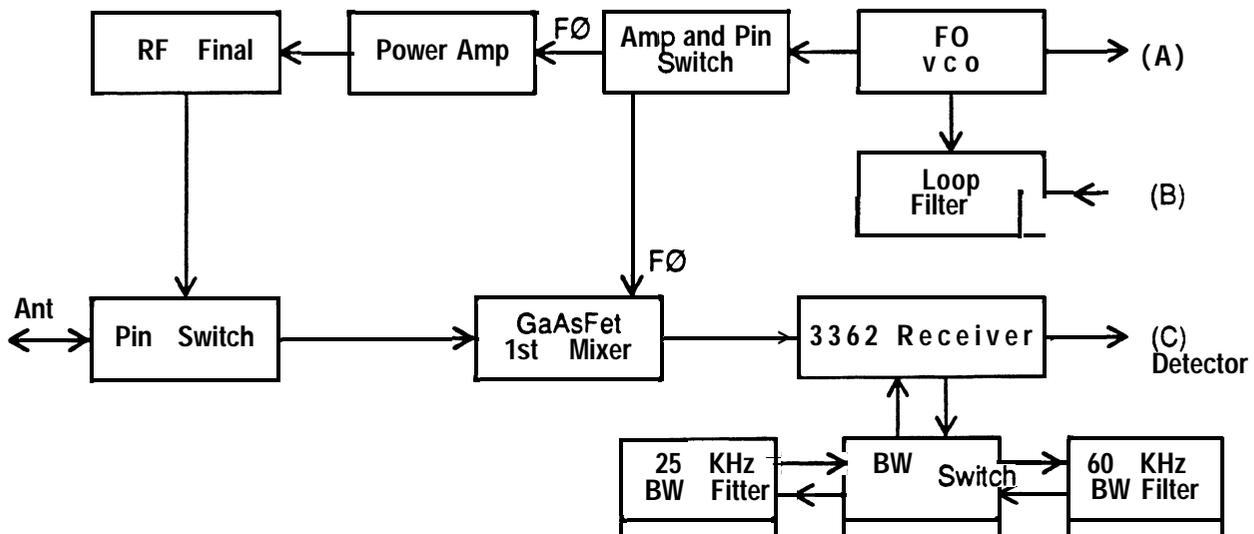
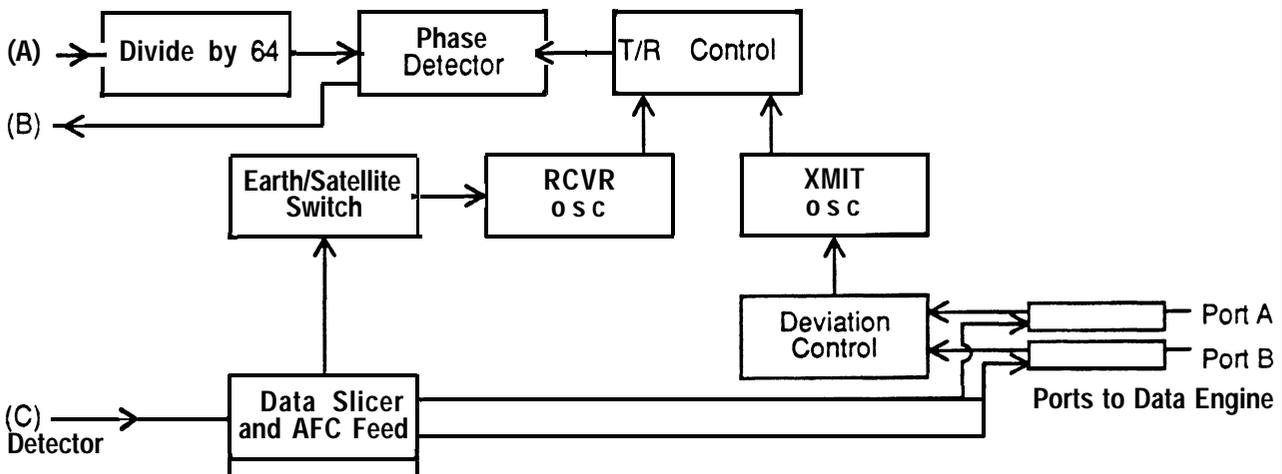


Figure 2 - DVR 4-2 Oscillators, AFC and Data Modulators



operational. In the narrow position, a Murata CFW455C is being used in the prototype at this point, providing a 6dB bandwidth of +/-12 KHz. In the wide position, a discrete stagger-tuned 60 KHz BW linear phase filter is configured. An analog switch is utilized to switch between these filters.

Now consider Figure 2 which includes frequency loop and TR control, AFC control, and modulation/demodulation data port circuits. The oscillator for the first mixer and the transmitter is derived from a loop consisting of receive and transmit crystal oscillators, digital phase detector, a divide by 64 counter, loop filter, the VCO (shown in Figure 1), and offset adjust potentiometers. The VCO

frequency will be 45 MHz below the selected UHF operational frequency during reception, set to 64 times the receive crystal oscillator frequency. When PTT is asserted, the VCO frequency will shift to 64 times the transmit crystal oscillator frequency. Loop characteristics are such that TR switching is kept below 5 ms. One potentiometer per crystal oscillator was added and set to provide a control voltage for the VCO, via an analog switch, such that the loop error voltage is small for a given crystal frequency selected, providing quick lock when TR switching.

For satellite use, automatic frequency control (AFC) was added, allowing for automatic tracking of signals received with a doppler

frequency shift. The AFC receive mode is activated by setting the 'terrestrial/satellite' (T/S) front panel switch to the S position. The control voltage for AFC is derived from the discriminator output and the LO will track the average frequency of the received signal.

The modulation and demodulation functions of the DVR 4-2 are denoted at the bottom of Figure 2. From the left, the output of the receive detector feeds the data slicer. AFC control is also derived here as described above. Raw discriminator (detector) output is fed to data port A, pin for pin compatible with the DVR 2-2 DB-9 connector port. For 19,200 baud wide bandwidth operation, the output of the data slicer is converted to a TTL level and then fed to port B for interfacing to the Data Engine (TNC). A data receive clock is not generated and data scramblers for transmit and receive are not provided; these functions are assigned to the modems or partial modems that would plug inside the Data Engine or other high-speed capable TNC.

Three forms of modulation are provided for within the block labeled deviation control. As with the DVR 2-2, one may use a standard mic or the 'DVR 2-2' data interface with port A a 50 mv p-p 'IX audio signal applied at port A will result in an FM signal with +/-3 KHz deviation. Port B is considered the high-speed port. A TTL TX signal applied there will generate an FM signal with +/-9600 KHz deviation. It is assumed that the 19,200 data source will be NRZ.

Intended Applications

It is anticipated, as per the requests for a wide bandwidth transceiver, that such units

would be used in UHF backbone networks, probably in conjunction with packet switches. Figure 3 describes one possible implementation in conjunction with the high-speed capable Data Engine.

The Data Engine is shown at the left and would include a G8BPQ packet switch EPROM, a DE9600/G3RUH modem and a DE19200 clock/scrambler. A DVR 2-2 would be attached to port 1 of the Data Engine to provide 9600 2-meter operation. The DVR 4-2 would be configured for wide bandwidth operation and attached to port 2 of the Data Engine. The DE19200 clock/scrambler board would plug inside the Data Engine and provides for transmit clock, receive clock recovery and optional scrambler operation.

With the G8BPQ EPROM installed and set in multi-drop KISS mode, two more ports, each at say 1200 baud, could be added via a KPC-4 attached to the serial port of the Data Engine. The whole configuration would then provide two 1200 user access ports, one 9600 baud 2-meter backbone node and one 19200 70-cm backbone node.

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