A BIT ERROR RATE TESTER
FOR TESTING DIGITAL LINKS

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Introduction

With the availability of several link-level protocols such as TEXNET and NETROM, many packet groups are installing inter-city digital links. As AEA and GLB begin shipping their digital radios and the 56 kbps radio demonstrated at the Dayton Hamfest becomes available, more Amateurs will require a method of testing the performance of these digital radios. This paper presents a test circuit which can be used during initial installation of a digital link to enable the installers to fine tune the radio on site. This circuit temporarily replaces the TNC or control computer and allows the installers to listen to the data link to determine how well it is performing. It can also be used for bench testing digital radios and modems.

Bit Error Rate Testers

The performance of any digital radio receiver is tested by measuring its bit error rate (BER). The BER of a data system is the probability of not receiving the transmitted bit correctly. This is normally expressed in percent or decimal form. For example, a, system with a BER of l x 10-3 or 0.1% has the probability of receiving the transmitted bit incorrectly once in every 1000 bits. Bit error rate is measured by comparing the transmitted data bits with the received data bits and counting the number of bit errors.

A block diagram of a straight-forward bit error rate tester (BERT) is shown in figure 1. A pseudo-noise (P-N) generator is used to generate a random data stream which is then sent to the modulator and over the channel to the demodulator. The P-N data is also sent to a delay box. The delay box is used to line up the data received from the demodulator with the transmitted data. Every modulator, channel and demodulator will have some delay due to the filters used in each. The transmitted and received data streams are then compared and the errors counted in a counter. Common implementations of BERTs use an XOR gate as the comparison elements which gives a high output when an error occurs. In order to count two errors in a row, the XOR output is usually ANDed with the data clock to give a transition to the counter for every error made. The delay element is usually made up of D flip-flops which are clocked at some multiple of the data clock. The higher clock allows for incremental adjustment of the transmit data stream since the delay of the data system may not be in whole bit increments. The P-N generator is probably the most unfamiliar part of a BERT to most Amateurs. This circuit is similar to an oscillator in a radio. As in an oscillator, the P-N generator has a feedback element which has delay and produces the P-N data stream. In digital circuits D flip-flops are used as delay elements.

A- block diagram of a P-N generator is shown in figure 2. The delayed data is combined in an XOR gate and the resulting bit is sent back to the input of the delay stages forming the feedback path. The data rate of the P-N generator is determined by the clock which clocks the delay stages. A P-N generator is called a pseudo-noise generator because it does not exactly produce a true noise output since once a P-N generator is started it is possible to determine the bit pattern it will generate. BY selecting a P-N generator with a long bit pattern, a sufficiently noise like output will be generated. The length of the P-N pattern is determined by the length of the delay element in the P-N generator. The length of the generated bit pattern will be (2 to the N) -1 where N is the number of delay elements (D flip-flops). For example, a P-N generator with 17 stages will produce a bit pattern 131071 bits long. At 9600 bps it will take over 13 seconds to repeat this pattern which is a long and suitably random pattern for any BER tests we may wish to do.

Although the BERT shown in the block diagram of figure 1 is excellent for bench tests, it has one major flaw which excludes it from being used to tune up links. That is it requires the transmit data stream to compare to the received data stream in order to count errors. What is needed is a way of transmitting random data over the link but still have a method of counting the BER at the receiver without the knowledge of all the individual transmitted bits.

An Alternative BERT

BY adding an XOR gate to the P-N generator as shown in figure 3, it can be seen that the bit pattern generated by this circuit is the same as that generated by the original P-N generator since a low on one input of an XOR gate will give the same data out as put in. If the low is now removed and that XOR input is connected to another data stream, the resulting circuit is a randomizer which is used in many modems to scramble-up the data in order to reduce the low frequency content of the data being sent. In other words, a P-N generator can also be looked at as a randomizer with just a one or a zero for the data input. This means we can send a P-N data stream over the test link and at the receiver build an un-randomizing circuit to get the original one (or zero) back again. We can then count the amount of zeros (or ones) we receive at the output of the un-randomizer and have the BER of the test link.

A block diagram of the un-randomizer is shown in figure 4. The un-randomizer contains a delay register the same length as the P-N generator and also contains an XOR gate, but the circuit is connected in an open loop configuration instead of a feedback loop. To show that the un-randomizer does indeed give a one output when a randomized one is being sent over the test link, we can go through the equations of the randomizer and un-randomizer. If we say the output of the Ath delay element of the randomizer is R(A) and the output of the Bth delay element is R(B). Then the output of the randomizer is:

$$R(A) \oplus R(B) \oplus 1 = R$$

If we say that the channel data bits are denoted by C, the Ath delay channel bit at the un-randomizer is C(A), and the Bth delay channel bit is C(B), then the output of the un-randomizer is:

$$C(A) \oplus C(B) \oplus C = D$$

We can see that C=R since the randomizer delay elements are just delaying the channel data bits. Therefore, at the output of the un-randomizer:

$$R(A) \oplus R(B) \oplus R = D$$

If we replace R with the output of the randomizer we get:

$$R(A) \oplus R(B) \oplus R(A) \oplus R(B) \oplus 1 = D$$

Since any data XORed with itself is zero, we see that D = 1.

BY similar arguments, we can prove that if a zero is randomized a zero will be output from the un-randomizer. We can also show that if the data in the channel is inverted, the resulting un-randomizer output will be inverted from the original data sent.

A schematic of the resulting BERT is shown in figure 5. U1 is a bit rate generator which contains an oscillator and dividers to obtain several data rates. If you are only going to operate at one data rate, you may want to replace this circuit with a fixed oscillator and dividers. A 16 times clock is required for the internal clock recovery circuit. U2 and u3 form the internal clock recovery circuit. In transmit this circuit gives a data clock to the P-N generator. In receive a clock is derived from the receive data to operate the un-randomizer. The receive clock is brought out to a test pin on the pannel to allow the connection of an oscilliscope to observe the receive eye pattern in the modem. An external clock input is proved for in receive for the case where the modem has a receive data clock output. u5 is the delay register for the P-N generator and un-randomizer. A 1.7 stage P-N generator was selected (1). U6 switches the circuit from a P-N generator in transmit to an un-randomizer in receive. U4 provides the XOR gates for the P-N/un-randomizer and also allows the data and external clock to be inverted. U7 provides retiming of the receive data and insures there are no timing problems in the P-N generator design. U8 re-times the un-randomized output. U9 ANDs the re-timed randomizer output with the receive clock to provide an error count output for the counter.

U10 is an audio amplifier. The re-timed output of the un-randomizer is sent to the audio amplifier to allow the data channel to be listened too. When noise is being received at the receiver, noise will be output at the un-randomizer output and can be heard in the speaker. When an error free signal is received, a zero will be put out of the re-timed un-randomizer and quiet will be heard in the speaker. For any error received a pop will be heard in the speaker. Therefore, to tune up the digital link, the installer would tune the radio for best noise quieting just as is done on a FM radio receiving a carrier.

Initial Tests

The BERT can be built in about a night using wire-wrap techniques. Once built, connect a counter to the counter output and set the data rate to 9600 bps. Put the Tx/Rx switch in the Tx position. Noise should be heard coming from the speaker. This is the P-N data being generated. If no noise is heard, put the DATA/m switch in the DATA position and switch the Tx/Rx switch to Rx and then back to Tx. Noise should now be coming from the speaker. The P-N generator has a problem in that it can lock up in an all ones state. Switching momentarily to Rx puts a zero in the delay register and forces it to start generating a pattern. Switch the Tx/Rx switch to Rx. Put the counter in a one second gate mode and it should read 9600. This is due to the un-randomizer filling up with all zeros and putting out a zero all the time. In one second you will get 9600 bits and in this case they are all wrong since the BERT is expecting a one to be sent. Put the DATA/$\overline{\text{DATA}}$ switch to $\overline{\text{DATA}}$ and the counter should read zero. In this case the un-randomizer has filled with all ones and is putting out a one so no errors are counted. Put the Tx/Rx switch into Tx and make sure noise is heard from the speaker. If no noise is heard restart the P-N source by again switching the DATA/$\overline{\text{DATA}}$ switch to DATA and switching the Tx/Rx switch to Rx and back to Tx. The counter should now read about 4800 since the error output is now looking at the random data that would be sent over the channel. You will not get 4800 exactly every time but if you would average a lot of readings the average should come close to 4800.

A Note on Freauencv Counters

I have used many commercial frequency counters, such as the Fluke 1953A and HP 5335A with this BERT without any problems. Unfortunately, I have also had to modify some counters to get them to work properly with this BERT. As an example, I modified a Ramsey CT-90 by running the error count output of the BERT directly to pin 28 of the Intersil 7216D used in the CT-90.

Using the BERT for Link Tests

For actual link tests you will need two BERTs. One at the transmitter site and one at the receiver site. The receive site should connect to the receive modem and verify that noise is heard with no signal. The transmitter should then go on the air and verify that the P-N generator is operating by listening for noise in the BERT speaker. The receiving BERT should quiet when the transmitter comes on the air. Any pops heard at that point are now errors. Since you obtain instant feedback as to when an error occurs, you can now do tests to see where the errors are coming from or tune the radio for least errors.

Actual BER tests of the link can be done by connecting a counter and counting the number of errors received. The bit error rate can then be computed. The BER is:

$$BER = \frac{\text{Number of Errors Counted}}{\text{Bit Rate X Counter Gate Time X 3}}$$

The factor of three in the denominator of the BER equation is due to the fact that every channel error that comes in is used three times in BERT. It is used once when it first comes in and is then used again when it gets to R(A) and then again when it gets to R(B). This three times error multiplication must be divided out to get the actual channel error rate. The three times error correction is valid for channel error rates of 1% or less.

As an example of calculating the channel bit error rate, if the link is operating at 9600 bps and the counter gate is ten seconds and 288 errors were counted, the BER is 288/(9600 X 10 X 3) or 0.1%.

By listening to the speaker output for different BER, you will eventually be able to have an idea what the BER is just from the speaker output. Using these techniques you can measure the margin of your digital links.

9.6 and 56 kbps modems

Those groups that have the TAPR 9600 bps modem (2) or use the 56 kbps modem shown at Dayton will not have to build all the circuitry shown in figure 5. These modems already contain the 17 stage randomizer and un-randomizer so all that is needed at the transmit side is a 16 times clock and a high input to the transmit data input. At the receive side, all that is needed to listen to the link is an audio amplifier. I have used Radio Shack catalog number 277-10088 amplifier with a 47 k resistor between the receive data out and the audio amplifier input. To actually measure the BER you would need the circuitry shown to the right of the dotted line on figure 5. In calculating the BER for these modems, the three times error multiplication should not be divided out, since this error multiplication is in the modem.

Additional Uses for the BERT

Two BERTs can be used to test the turn around time of digital radios. By observing the data out of the un-randomizer on the receiving BERT on one channel of an oscilliscope and triggering the oscilliscope on the transmit line of the transmitter, the time from scope trigger to the point when all ones are coming out of the un-randomizer is the turn around time of the transmitter.

The receiver recovery time can be measured by transmitting continuously a P-N sequence and observing the output of the receive un-randomizer on an oscilliscope triggered on the release of the transmit line. The time from scope trigger to the point when all ones are coming out of the un-randomizer is the turn around time of the receiver.

The P-N generator can be used as a noise source for doing audio tests as can be heard in the speaker of the BERT. This noise source can be used to test HF modems. Since our present HF modems are audio modems transmitted using linear (SSB) techniques, an audio test using three BERTs could be performed (4).

Conclusions

A bit error rate tester has been described which allows installers of digital links to listen to the quality of the link and measure bit error rate of the link. This BERT can also be used for bench testing future data modems or for more accurate testing of existing modems. Quantitative tests comparing various modems can be done using this BERT.

An attempt was also made to explain the operation of a P-N generator.

Acknowledgements

I would like to thank Bruce Eastmond, K9LAY for thinking of listening to the error output of BERT. Thanks also go once again to Paul Newland, AD71 for providing the state machine code used in the clock recovery circuit.

References

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2) S. Goode, K9NG, "The Bit Error Rate Performance of the TAPR TNC Modem", QEX #18, August 1983.

3) S. Goode, K9NG, "Modifying the Hamtronics FM-5 for 9600 BPS Packet Operation", Fourth ARRL Amateur Radio Computer Networking Conference, San Francisco, Ca., March 30, 1985.

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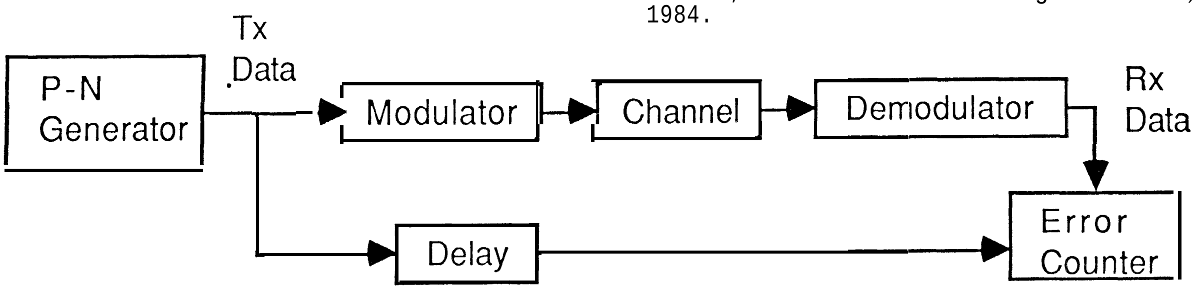

Figure 1
Bit Error Rate Tester

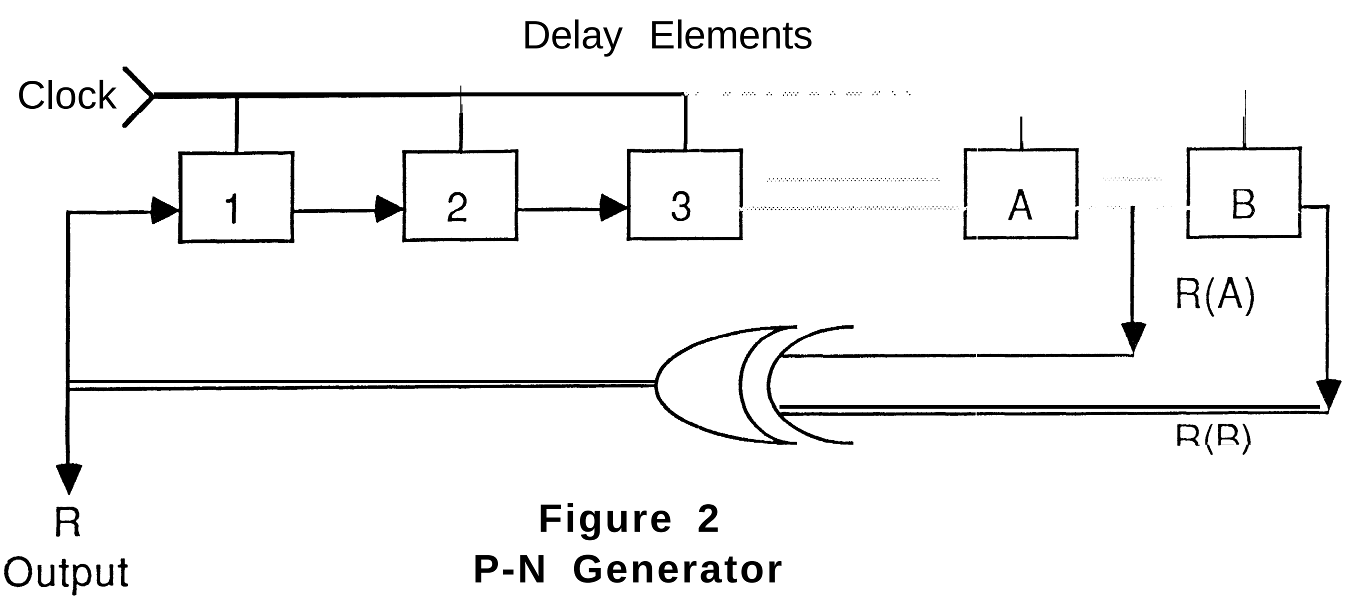

Figure 2
P-N Generator

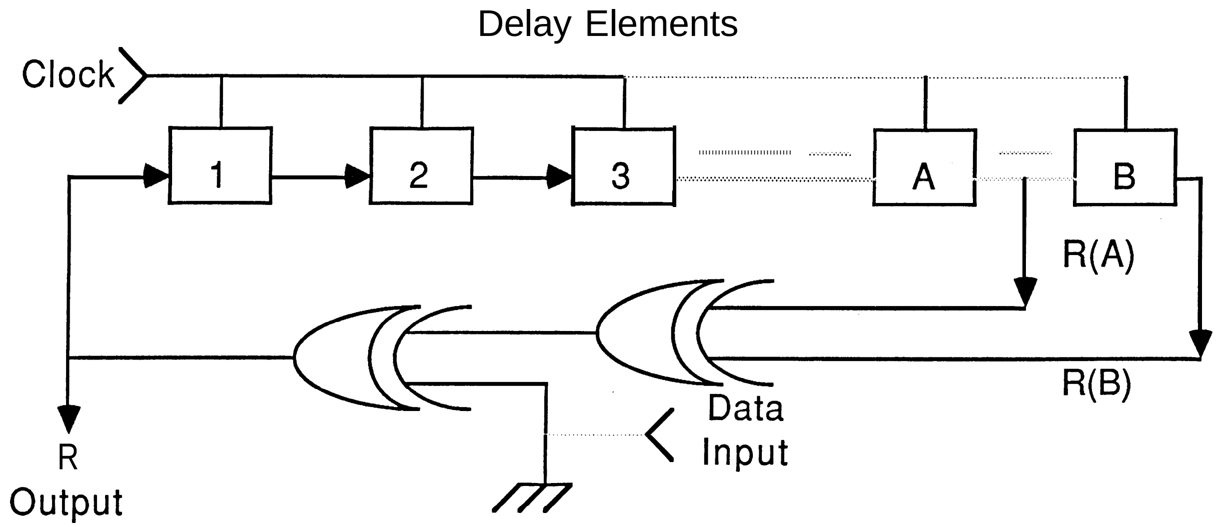

Figure 3
Randomizer

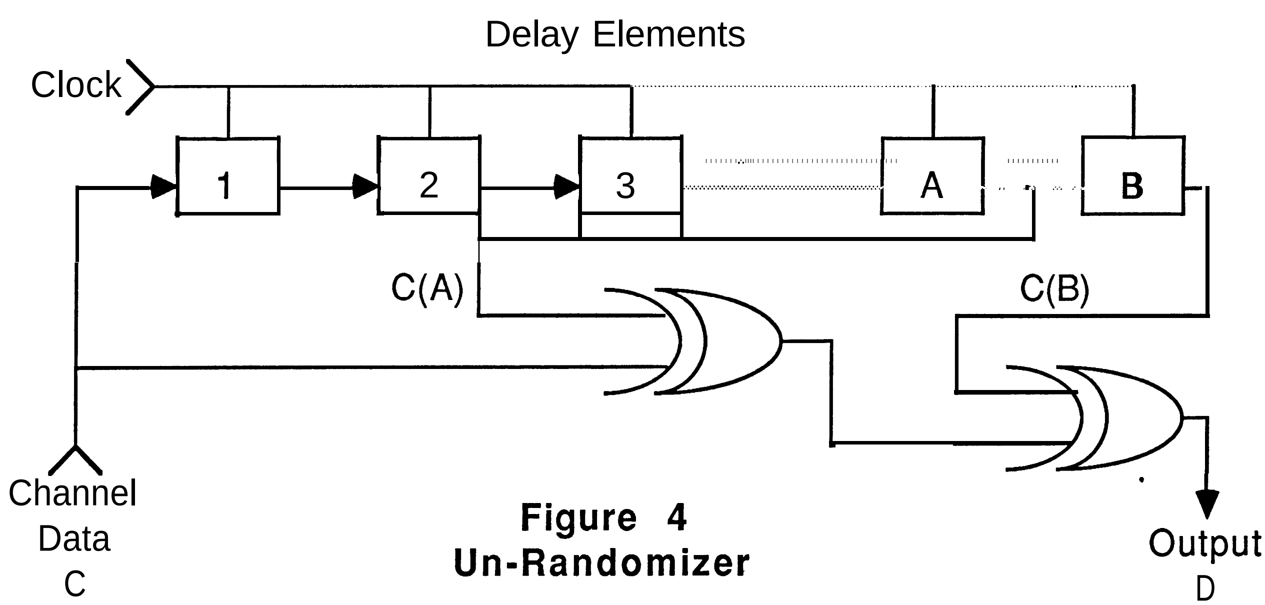

Figure 4
Un-Randomizer

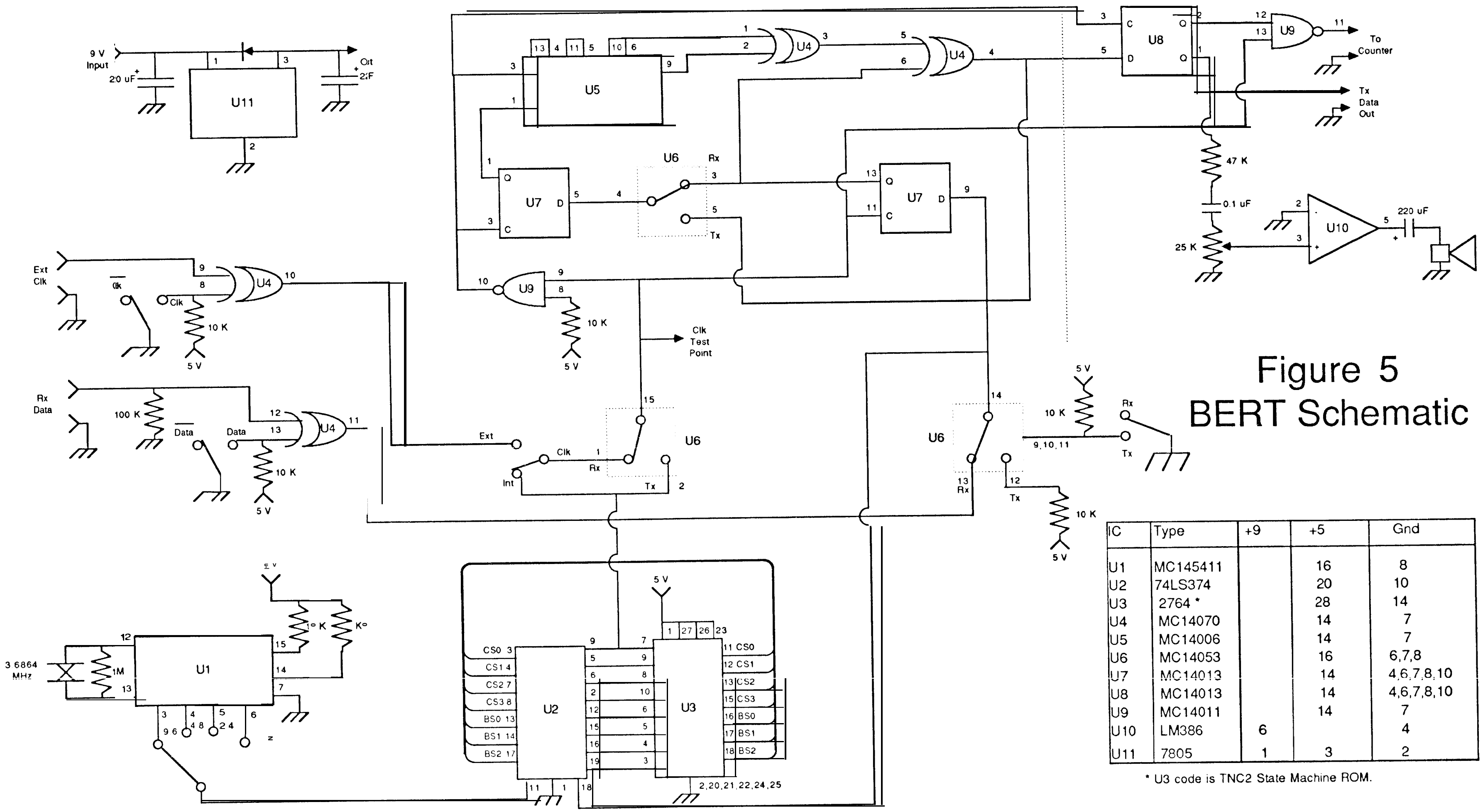

Figure 5
BERT Schematic

IC	Type	+9	+5	Gnd
U1	MC145411		16	8
U2	74LS374		20	10
U3	2764 *		28	14
U4	MC14070		14	7
U5	MC14006		14	7
U6	MC14053		16	6,7,8
U7	MC14013		14	4,6,7,8,10
U8	MC14013		14	4,6,7,8,10
U9	MC14011		14	7
U10	LM386	6		4
U11	7805	1	3	2

* U3 code is TNC2 State Machine ROM.